DAQ

PC-DIO-24/PnP User Manual

24-bit Digital I/O Board for ISA Computers

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This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Notice to User: ***Changes or modifications not expressly approved by National Instruments could void the user's authority to operate the equipment under the FCC Rules.***

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Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

Cet appareil numérique de la classe A respecte toutes les exigences du Règlement sur le matériel brouilleur du Canada.

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This manual describes the mechanical and electrical aspects of the PC-DIO-24/PnP and contains information concerning its operation and programming.

The PC-DIO-24/PnP is a member of the National Instruments family of I/O channel expansion boards for ISA computers. These boards are designed for high-performance, low-cost data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

This manual applies to the PC-DIO-24PnP and to the PC-DIO-24, a non-Plug and Play device. The boards are identical except for the differences listed in Appendix D, *Using Your PC-DIO-24 (Non-PnP) Board*.

Organization of This Manual

The *PC-DIO-24/PnP User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the PC-DIO-24/PnP, lists what you need to get started, describes software programming choices, optional equipment, and custom cables, and explains how to unpack the PC-DIO-24/PnP.
- Chapter 2, *Installation and Configuration*, describes how to install and configure the PC-DIO-24/PnP.
- Chapter 3, *Signal Connections*, includes timing specifications and signal connection instructions for the PC-DIO-24/PnP I/O connector.
- Chapter 4, *Theory of Operation*, contains a functional overview of the PC-DIO-24/PnP board and explains the operation of each functional unit making up the PC-DIO-24/PnP.
- Appendix A, *Specifications*, lists the specifications for the PC-DIO-24/PnP board.
- Appendix B, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI Semiconductor 82C55A CMOS PPI.

- Appendix C, *Register-Level Programming*, describes in detail the address and function of each of the PC-DIO-24/PnP control and status registers.
- Appendix D, *Using Your PC-DIO-24 (Non-PnP) Board*, describes the differences between the PC-DIO-24 and PC-DIO-24PnP boards, the PC-DIO-24 board configuration, and the PC-DIO-24 installation into your computer.
- Appendix E, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.
- The *Index* alphabetically lists the topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

This icon to the left of bold italicized text denotes a note, which alerts you to important information.

This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

82C55A — 82C55A refers to the OKI Semiconductor 82C55A CMOS PPI.

<> — Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit or signal name (for example, PB<7..0>).

bold — Bold text denotes the names of menus, menu items, parameters, dialog boxes, dialog box buttons or options, icons, windows, Windows 95 tabs, or LEDs.

bold italic — Bold italic text denotes a note, caution, or warning.

italic — Italic text denotes emphasis, a cross reference, or an introduction to a key concept.

`monospace`	Text in this font denotes text or characters that you should enter literally from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and for statements and comments taken from programs.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC	PC refers to the IBM PC/XT, the IBM PC AT, and compatible ISA bus computers unless otherwise noted.
PC-DIO-24/PnP	PC-DIO-24/PnP refers to both the Plug and Play and non-Plug and Play compatible versions of the board.
PC-DIO-24PnP	PC-DIO-24PnP refers to the Plug and Play version of the board.
PC-DIO-24	PC-DIO-24 refers to the non-Plug and Play version of the board.
PnP	PnP (Plug and Play) refers to a device that is fully compatible with the industry standard Plug and Play ISA Specification.
non-PnP	Non-PnP refers to a device that requires you to configure the device base address and interrupt level with switches and jumpers. You must perform this configuration before installing the product in the computer.
PPI	PPI (programmable peripheral interface) is the DIO chip on the PC-DIO-24/PnP board.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.

National Instruments Documentation

The *PC-DIO-24/PnP User Manual* is one piece of the documentation set for your data acquisition (DAQ) system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the different types of manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows/CVI manual sets and the NI-DAQ documentation. After you set up your hardware system, use either the application software documentation or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis Manual*—Read this manual for maintenance information on the chassis and for installation instructions.

Related Documentation

The following documents contain information that you may find helpful as you read this manual:

- Your computer technical reference manual
- *Plug and Play ISA Specification*

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix E, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the PC-DIO-24/PnP, lists what you need to get started, describes software programming choices, optional equipment, and custom cables, and explains how to unpack the PC-DIO-24/PnP.

About the PC-DIO-24/PnP

Thank you for purchasing the National Instruments PC-DIO-24/PnP. The PC-DIO-24/PnP is a low cost, 24-bit, parallel digital I/O interface for ISA computers. An OKI 82C55A programmable peripheral interface (PPI) chip controls the 24 bits of digital I/O. The 82C55A chip is very flexible and powerful when interfacing with peripheral equipment, can operate in either a unidirectional or bidirectional bus mode, and can generate interrupt requests to the host computer. You can program the 82C55A chip for numerous 8-bit, 16-bit, or 24-bit digital I/O applications. All digital I/O communication is through a standard 50-pin male connector. The pin assignments for this connector are compatible with standard 24-channel digital I/O applications.

PnP refers to the Plug and Play technology used in this board. See the definition in the *Glossary* for an explanation. If you have the non-PnP version of the PC-DIO-24/PnP, see Appendix D, *Using Your PC-DIO-24 (Non-PnP) Board*, for the differences between the PnP version and the non-PnP version.

You can use the PC-DIO-24/PnP in a wide range of digital I/O applications. With the PC-DIO-24/PnP, you can use your PC as a digital I/O system controller for laboratory testing, production testing, and industrial process monitoring and control.

Detailed specifications of the PC-DIO-24/PnP are in Appendix A, *Specifications.*

What You Need to Get Started

To set up and use your PC-DIO-24/PnP, you will need the following:

- ❑ PC-DIO-24PnP or PC-DIO-24 board
- ❑ *PC-DIO-24/PnP User Manual*
- ❑ One of the following software packages and documentation:

  BridgeVIEW
  ComponentWorks
  LabVIEW for Windows
  LabWindows/CVI
  Measure
  NI-DAQ for PC compatibles
  VirtualBench

- ❑ Your computer

Software Programming Choices

You have several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software, NI-DAQ, or register-level programming.

National Instruments Application Software

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

LabVIEW features interactive graphics and a state-of-the-art user interface and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

LabWindows/CVI features interactive graphics and a state-of-the-art user interface and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using ComponentWorks, LabVIEW, LabWindows/CVI, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation, digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ also internally addresses many of the complex issues between the computer and the plug-in device, such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Figure 1-1 illustrates the relationship between NI-DAQ and your National Instruments application software.

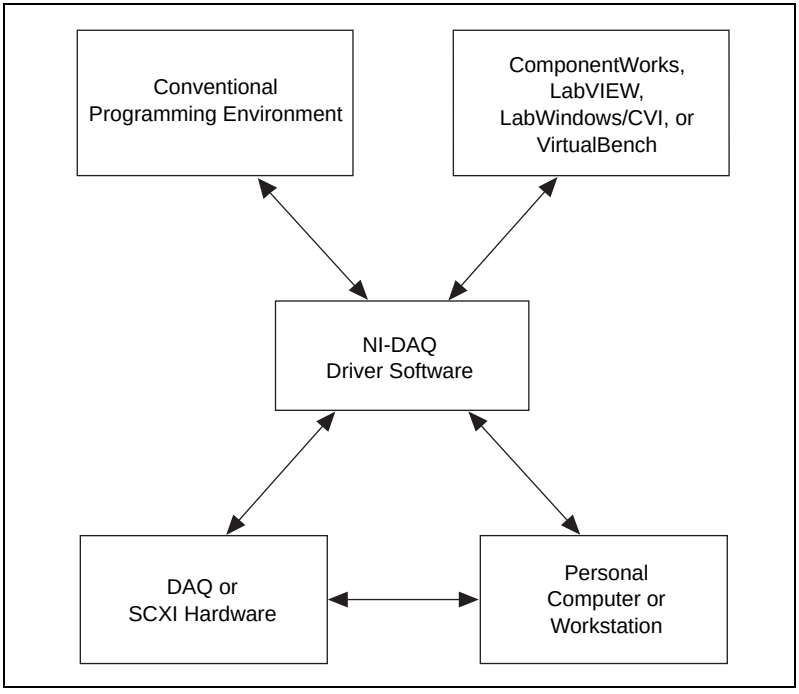


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using National Instruments application software to program your National Instruments DAQ hardware. Using the National Instruments application software is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your PC-DIO-24/PnP board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel-count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays.

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

☞ **Note:** ***The PC-DIO-24/PnP can drive the SSR-ODC-5 output module and all SSR input modules available from National Instruments, but cannot reliably sink sufficient current to drive the SSR-OAC-5 and SSR-OAC-5A output modules.***

To drive a SSR-OAC-5 or SSR-OAC-5A, you can either use a non-inverting digital buffer chip between the PC-DIO-24/PnP and the SSR backplane, or use another National Instruments board with higher drive current.

Custom Cables

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful.

The PC-DIO-24/PnP I/O connector is a 50-pin male ribbon-cable header. The manufacturer part numbers used by National Instruments for this header are as follows:

- Electronic Products Division/3M (part number 2550-5002)
- T&B/Ansley Corporation (part number 609-5007)

The mating connector for the PC-DIO-24/PnP is a 50-position, polarized, ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the PC-DIO-24/PnP. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 622-5041)

The standard ribbon cables (50-conductor, 28 AWG, stranded) that can be used with these connectors are as follows:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

Recommended manufacturer part numbers for the 50-pin edge connector for connecting to a module rack with an edge connector are as follows:

- Electronic Products Division/3M (part number 3415-0001)
- T&B Ansley Corporation (part number 622-5015)

A polarizing key can be plugged into these edge connectors to prevent inadvertent upside-down connection to the I/O module rack. The location of this key varies from rack to rack. Consult the specification for the rack you intend to use for the location of any polarizing key. The recommended manufacturer part numbers for this polarizing key are as follows:

- Electronic Products Division/3M (part number 3439-2)
- T&B Ansley Corporation (part number 622-0005)

Unpacking

Your PC-DIO-24/PnP board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your PC chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch exposed connector pins.

Installation and Configuration

Chapter 2

This chapter describes how to install and configure the PC-DIO-24/PnP.

Installation

Note: ***Install your driver software before installing your hardware. Refer to your NI-DAQ release notes for software installation instructions.***

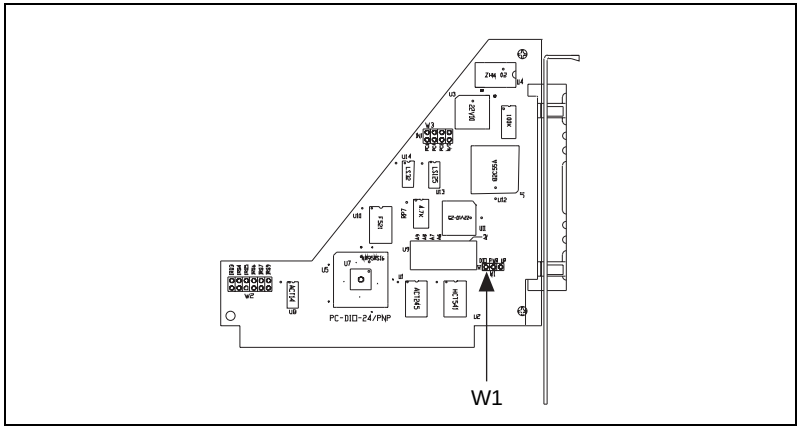


Figure 2-1. Jumper W1 Location

Note: ***The PC-DIO-24/PnP uses 100 kΩ resistors for polarity selection at power-up. You can use jumper W1 to select whether data signals are pulled up to Vcc (+5 VDC), factory default, or pulled down to GND. Figure 2-1 shows jumper W1. For more information, see the*** *Digital I/O Power-up State Selection* ***section in Chapter 3,*** *Signal Connections.*

You can install the PC-DIO-24/PnP in any unused 8- or 16-bit expansion slot in your computer. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Turn off and unplug your computer.
2. Remove the I/O channel top cover or access port.
3. Remove the expansion slot cover on the computer back panel.
4. Insert the PC-DIO-24/PnP into any 8- or 16-bit slot. It may be a tight fit, but *do not* force the board into place.
5. Screw the PC-DIO-24/PnP mounting bracket to the computer back panel rail.
6. Visually verify the installation.
7. Replace the computer cover.
8. Plug in and turn on your computer.

The PC-DIO-24/PnP board is now installed.

Hardware Configuration

Plug and Play

The PC-DIO-24PnP is fully compatible with the industry-standard Intel/Microsoft Plug and Play Specification. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the PC-DIO-24PnP base I/O address and interrupt channel.

The Configuration Manager receives all of the resource requests at startup, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

Base I/O Address and Interrupt Selection

To change base I/O address or interrupt selection, refer to the NI-DAQ Configuration Utility Help file. You can configure the PC-DIO-24PnP to use base addresses in the range of 100 to 3E0 hex. Each board occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140…, 3E0 hex.

The PC-DIO-24PnP can use interrupt channel 3, 4, 5, 7, or 9.

☞ **Note:** ***To configure the non-Plug and Play PC-DIO-24 board, refer to Appendix D,*** *Using Your PC-DIO-24 (Non-PnP) Board.*

Chapter 3

Signal Connections

This chapter includes timing specifications and signal connection instructions for the PC-DIO-24/PnP I/O connector.

⚠ **Caution:** ***Connections that exceed any of the maximum ratings of input or output signals on the PC-DIO-24/PnP can damage the board and the PC. National Instruments is NOT liable for any damages resulting from any such signal connections. Maximum ratings for each signal are given in this chapter under the discussion of that signal.***

I/O Connector

Figure 3-1 shows the pin assignments for the PC-DIO-24/PnP digital I/O connector.

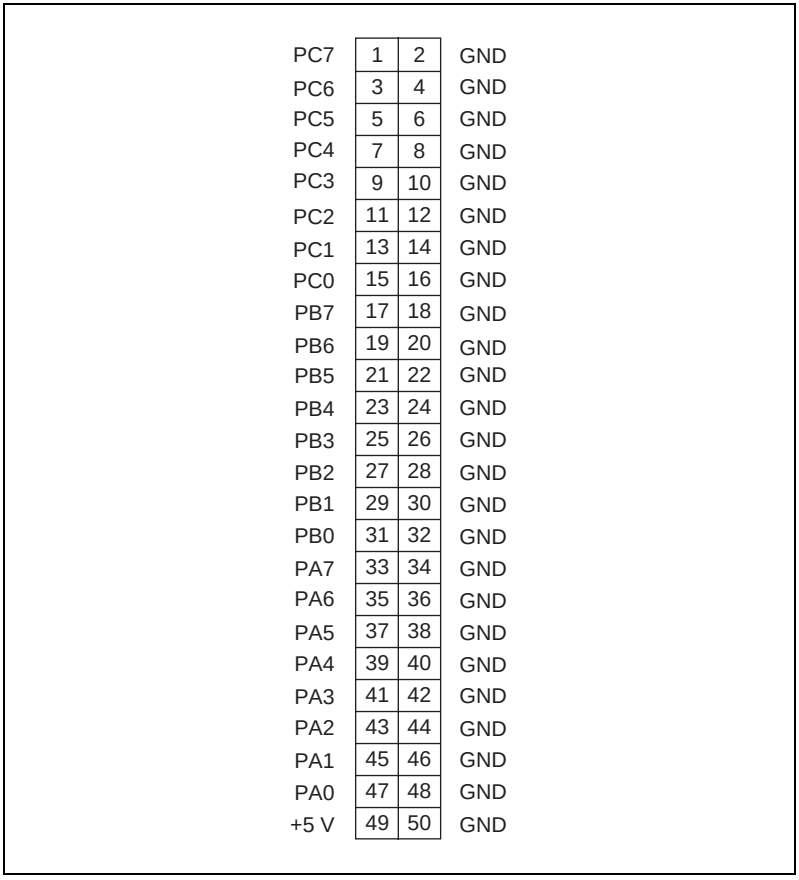


Figure 3-1. Digital I/O Connector Pin Assignments

Signal Descriptions

Table 3-1 describes the PC-DIO-24/PnP signals.

Table 3-1. Signal Descriptions

Pin	Signal Name	Description
1, 3, 5, 7, 9, 11, 13, 15	PC<7..0>	Port C—Bidirectional data lines for port C. PC7 is the MSB, PC0 the LSB.
17, 19, 21, 23, 25, 27, 29, 31	PB<7..0>	Port B—Bidirectional data lines for port B. PB7 is the MSB, PB0 the LSB.
33, 35, 37, 39, 41, 43, 45, 47	PA<7..0>	Port A—Bidirectional data lines for port B. PA7 is the MSB, PA0 the LSB.
49	+5 V	+5 Volts—This pin is fused for up to 1 A at +4.65 to 5.25 V.
All even-numbered pins	GND	Ground—These signals are connected to the computer ground reference.

The absolute maximum voltage input rating is –0.5 to +5.5 V with respect to GND.

Port C Pin Assignments

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is treated as one 8-bit I/O port. If port A or B is in mode 1 or 2, then some or all of the port C lines are used for status and handshaking signals. Any unused lines are available for general-purpose input and output. Table 3-2 summarizes the signal assignments of port C for each programmable mode. Ports A and B can be in different modes; the table does not show every possible combination. See Appendix C, *Register-Level Programming*, for register-level programming information.

Caution: ***During programming, note that each time you configure any port, output ports A and C are reset to 0, and output port B is undefined.***

Table 3-2. Port C Signal Assignments

Programming Mode	Group A				Group B			
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O

* Indicates that the signal is active low.

Digital I/O Signal Connections

The following specifications and ratings apply to the digital I/O lines. The maximum input logic high and output logic high voltages assume a Vcc supply voltage of 5.0 V.

The absolute maximum voltage rating is –0.5 to +5.5 V with respect to GND.

Digital input specifications (referenced to GND):

Input logic high voltage	2.2 V min	5.3 V max
Input logic low voltage	–0.3 V min	0.8 V max
Input high current (V_{in} = 5 V, W1 set to pullup)	—	11.0 µA max
Input high current (V_{in} = 5 V, W1 set to pulldown)	—	65 µA max
Input logic low current (V_{in} = 0 V, W1 set to pullup)	—	–65 µA max
Input logic low current (V_{in} = 0 V, W1 set to pulldown)	—	–11 µA max

Digital output specifications (referenced to GND):

Output logic high voltage (I_{ol} = –2.5 mA)	3.7 V min	5.0 V max
Output logic high voltage (I_{oh} = –4 mA)	2.7 V min	5.0 V max
Output logic low voltage (I_{ol} = 2.5 mA)	0 V min	0.4 V
Output logic low voltage (I_{ol} = 4 mA)	0 V min	0.5 V

Figure 3-2 depicts signal connections for three typical digital I/O applications.

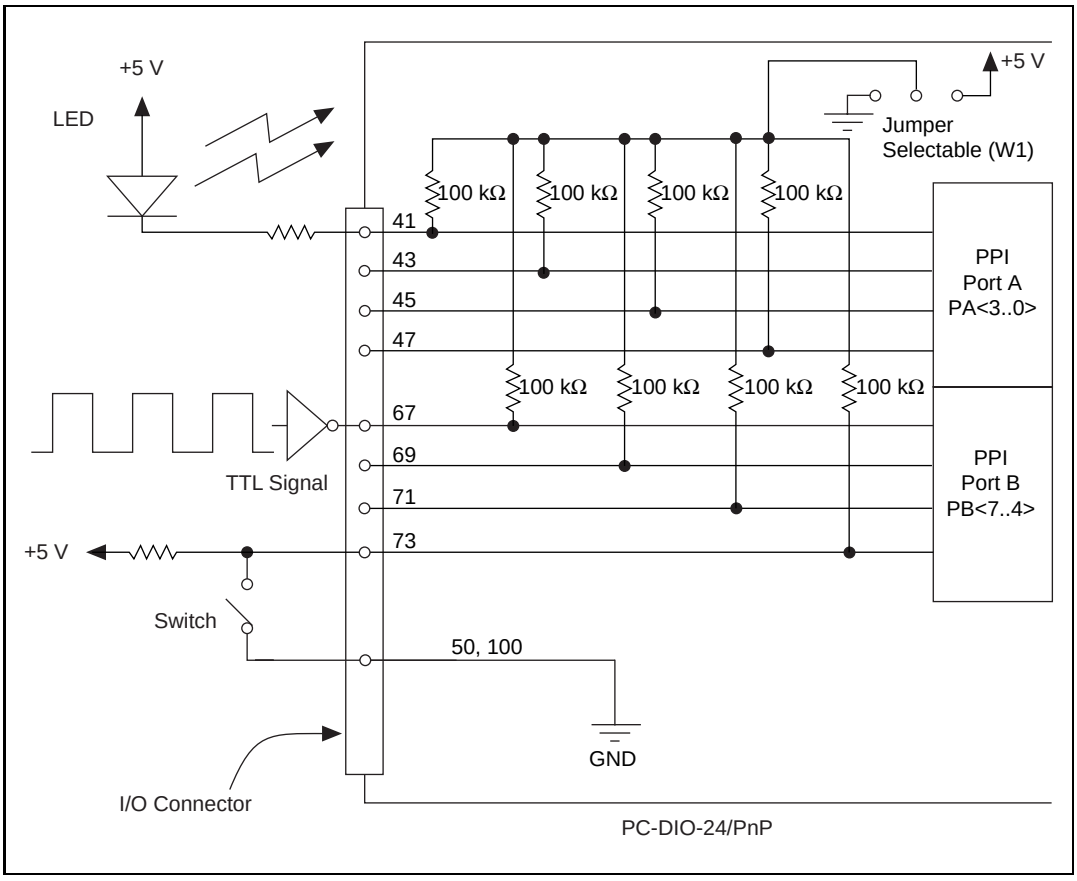


Figure 3-2. Digital I/O Connections

In Figure 3-2, port A is configured for digital output, and port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch in Figure 3-2. Digital output applications include sending TTL signals and driving external devices such as the LED shown in this figure.

Power Connections

Pin 49 of the I/O connector is connected to the +5 V supply from the PC power supply. This pin is referenced to GND and can be used to power external digital circuitry. This +5 V supply has a 1 A self-resetting protection fuse in series. Simply remove the circuit causing the heavy current load and the fuse will reset itself.

Power rating	1 A at +4.65 to 5.25 V

Caution: ***Under no circumstances should this +5 V power pin be connected directly to ground or to any other voltage source on the PC-DIO-24/PnP or any other device. Doing so may damage the PC-DIO-24/PnP and the PC. National Instruments is NOT liable for damage resulting from such a connection.***

Digital I/O Power-up State Selection

You can power up the PC-DIO-24/PnP digital I/O lines in a user-defined state. The PC-DIO-24/PnP facilitates user-configurable pull-up or pull-down. Each DIO channel is connected to a 100 kΩ resistor and can be pulled high or low using jumper W1. You can use W1 to pull all 24 DIO lines high or low. However, you may want to pull individual lines in different directions. To do this properly, you must understand the nature of the drive current on those lines and adhere to TTL logic levels.

High DIO Power-up State

If you select the pulled-high mode, each DIO line will be pulled to Vcc (approximately +5 VDC) with a 100 kΩ resistor. If you want to pull a specific line low, connect between that line and ground a pull-down resistor (R_L) whose value will give you a maximum of 0.4 VDC. Using the largest possible resistor ensures that you do not use more current than necessary to perform the pull-down task, and that the DIO can still drive the line. The DIO lines provide a maximum of 2.5 mA at 3.7 V in the high state.

Also, make sure the resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-up resistor drives the voltage at the resistor above a TTL low level of 0.4 VDC.

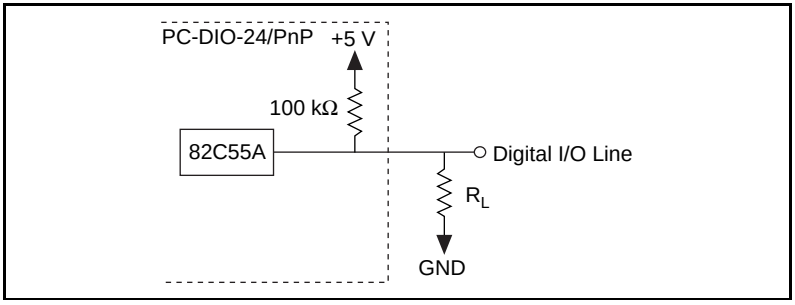


Figure 3-3. DIO Channel Configured for High DIO Power-up State with External Load

Example:
At power up, the board is configured for input and, by default, all DIO lines are high. To pull one channel low, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage.
2. Using the following formula, calculate the largest possible load to maintain a logic low level of 0.4 V with a minimum reduction to the DIO drive current.

   $V = I * R_L \Rightarrow R_L = V / I$, where:

   $V = 0.4$ V ; Voltage across R_L

   $I = 46\ \mu A + 11\ \mu A$; 4.6 V across the 100 kΩ pull-up resistor and 11 µA max leakage current

   Therefore:

   $R_L = 7.0$ kΩ ; 0.4 V / 57 µA

This resistor value, 7.0 kΩ, provides a maximum of 0.4 V on the DIO line at power up. You can substitute smaller resistor values to lower the voltage or to provide a margin for Vcc variations and other factors. However, smaller values will draw more current, leaving less drive current for other circuitry connected to this line. The 7.0 kΩ resistor reduces the amount of logic high source current by 0.4 mA with a 2.8 V output.

Low DIO Power-up State

If you select pulled-low mode, each DIO line will be pulled to GND (0 VDC) using a 100 kΩ resistor. To pull a specific line high, connect a pull-up resistor that will give you a minimum of 2.8 VDC. Using the largest possible resistance value ensures that you do not to use more current than necessary to perform the pull-up task, and that the DIO can still drive the line. The DIO lines are capable of sinking a maximum of 2.5 mA at 0.4 V in the low state.

Also, make sure the pull-up resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-down resistor brings the voltage at the resistor below a TTL high level of 2.8 VDC.

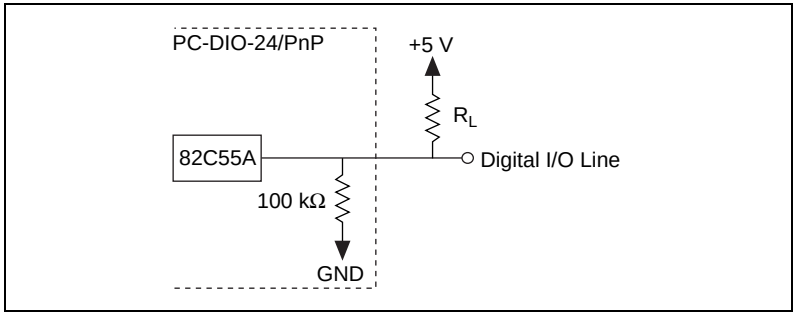


Figure 3-4. DIO Channel Configured for Low DIO Power-up State with External Load

Example:
At power up, the board is configured for input and jumper W1 is set in the low DIO power-up state, which means all DIO lines are pulled low. If you want to pull one channel high, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the higher the voltage.
2. Using the following formula, calculate the largest possible load to maintain a logic high level of 2.8 V and supply the maximum sink current.

   $V = I * R_L \Rightarrow R_L = V / I$, where:

   $V = 2.2$ V ; voltage across R_L

   $I = 28\ \mu A + 11\ \mu A$; 2.8 V across the 100 kΩ pull-up resistor and 11 μA max leakage current

Therefore:

$R_L = 5.6\ k\Omega$; 2.2 V / 39 µA

This resistor value, 5.6 kΩ, provides a minimum of 2.8 V on the DIO line at power up. You can substitute smaller resistor values but they will draw more current, leaving less sink current for other circuitry connected to this line. The 5.6 kΩ resistor will reduce the amount of a logic low sink current by 0.8 mA with a 0.4 V output.

Timing Specifications

This section lists the timing specifications for handshaking with the PC-DIO-24/PnP. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

The signals in Table 3-3 are used in the timing diagrams on the subsequent pages.

Table 3-3. Timing Signal Descriptions

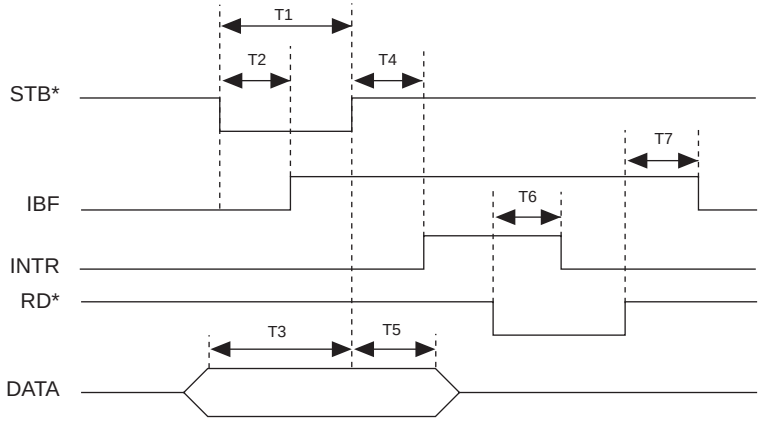
Name	Signal Direction	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the selected port has been accepted. This signal is a response from the external device that it has received the data from the PC-DIO-24/PnP.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written to the selected port.

Table 3-3. Timing Signal Descriptions (Continued)

Name	Signal Direction	Description
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A is requesting service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the control lines of the PC.
WR*	Internal	Write Signal—This signal is the write signal generated from the control lines of the PC.
DATA	Bidirectional	Data Lines at the Selected Port—This signal indicates when the data on the data lines at a selected port is available (output) or should be available (input).

Mode 1 Input Timing

The following figure illustrates the timing specifications for an input transfer in mode 1.



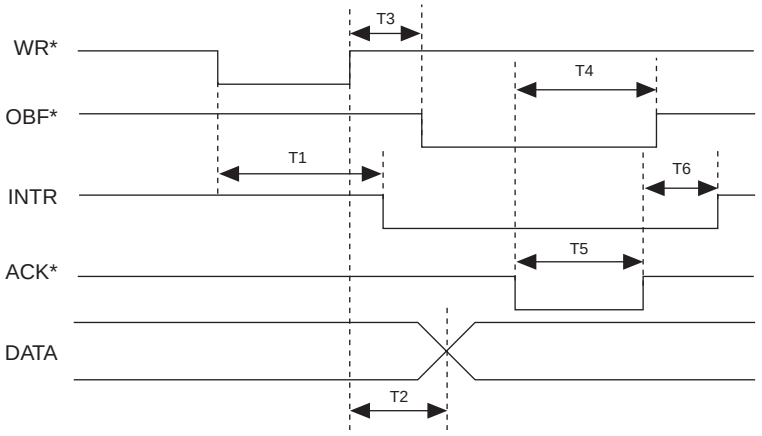
Name	Description	Minimum	Maximum
T1	STB* pulse width	100	—
T2	STB* = 0 to IBF* = 1	—	150
T3	Data before STB* = 1	20	—
T4	STB* = 1 to INTR = 1	—	150
T5	Data after STB* = 1	50	—
T6	RD* = 0 to INTR = 0	—	200
T7	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Figure 3-5. Mode 1 Timing Specification for Input Transfers

Mode 1 Output Timing

The following figure illustrates the timing specifications for an output transfer in mode 1.



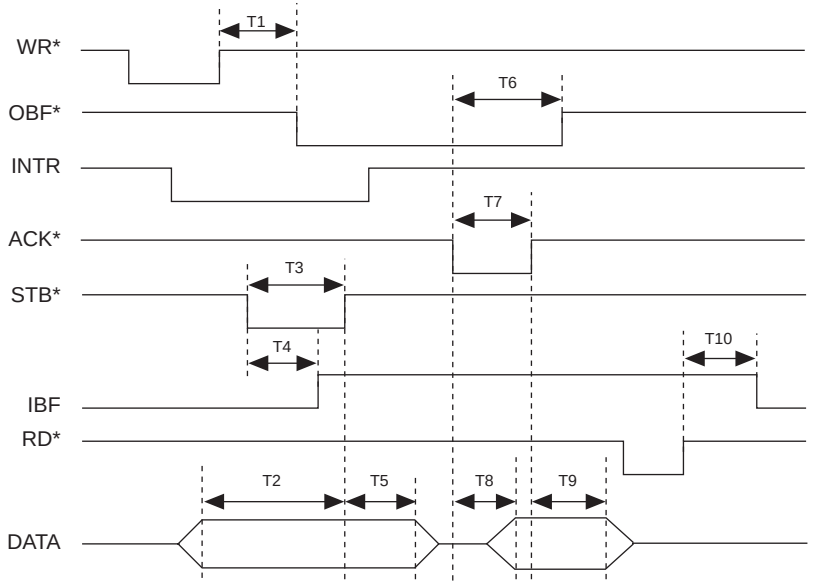
Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	—	250
T2	WR* = 1 to output	—	200
T3	WR* = 1 to OBF* = 0	—	150
T4	ACK* = 0 to OBF* = 1	—	150
T5	ACK* pulse width	100	—
T6	ACK* = 1 to INTR = 1	—	150

All timing values are in nanoseconds.

Figure 3-6. Mode 1 Timing Specification for Output Transfers

Mode 2 Bidirectional Timing

The following figure illustrates the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	—	150
T2	Data before STB*= 1	20	—
T3	STB* pulse width	100	—
T4	STB* = 0 to IBF = 1	—	150
T5	Data after STB* = 1	50	—
T6	ACK* = 0 to OBF = 1	—	150
T7	ACK* pulse width	100	—
T8	ACK* = 0 to output	—	150
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Figure 3-7. Mode 2 Timing Specification for Bidirectional Transfers

Chapter 4

Theory of Operation

This chapter contains a functional overview of the PC-DIO-24/PnP board and explains the operation of each functional unit making up the PC-DIO-24/PnP.

Functional Overview

The block diagram in Figure 4-1 illustrates the key functional components of the PC-DIO-24/PnP board.

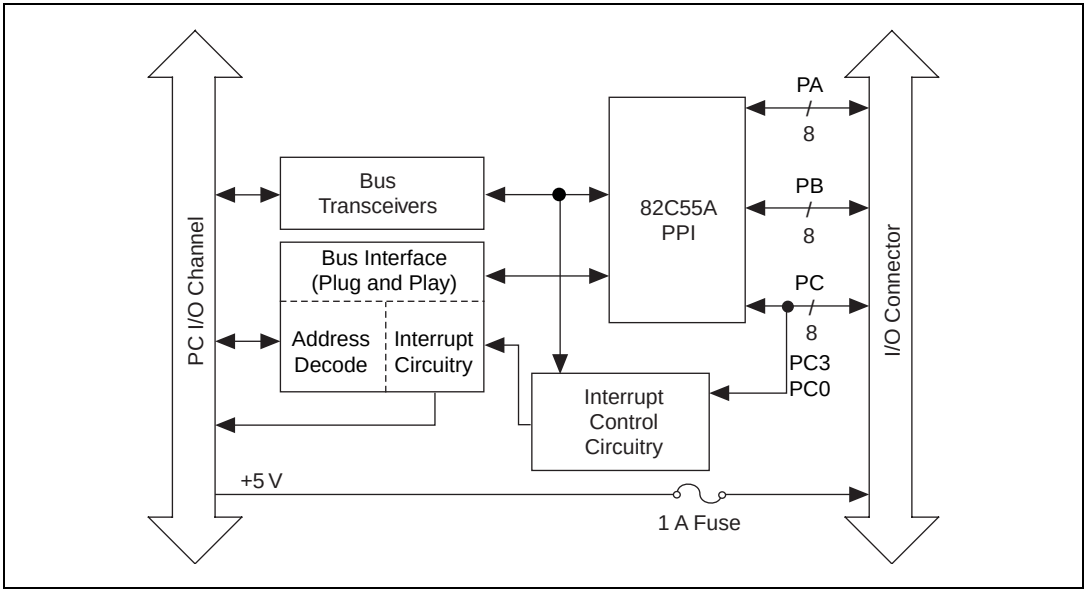


Figure 4-1. PC-DIO-24/PnP Block Diagram

The PC I/O channel consists of an address bus, a data bus, interrupt lines, and several control and support signals. Control and data transfers to the system microprocessor are asynchronous.

Bus Transceivers

The bus transceivers send and receive data lines and other signals to and from the PC I/O channel.

Bus Interface

The PC-DIO-24PnP Plug and Play circuitry automatically arbitrates and assigns system resources. Software performs all bus-related configuration, such as setting the board base address and interrupt level.

On the PC-DIO-24 (non-PnP), switches and jumpers set the board base address and interrupt level.

Interrupt Control Circuitry

The PC-DIO-24PnP interrupt channel is selected by the Plug and Play circuitry. Two software-controlled registers determine what sources, if any, can generate interrupts. The 82C55A device has two interrupt lines, PC3 and PC0, connected to the interrupt circuitry.

The PC-DIO-24 (non-PnP) uses one of the extra PC lines (jumper-selectable) as an interrupt enable.

82C55A Programmable Peripheral Interface

The 82C55A PPI chip is the heart of the PC-DIO-24/PnP. This chip has 24 programmable I/O pins that represent three 8-bit ports—PA, PB, and PC. You can program each port as an input or an output port. The 82C55A has three modes of operation—simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In mode 1, the three ports are divided into two groups—group A and group B. Each group has eight data bits and three control and status bits from port C (PC). Group A can also use mode 2. In mode 2, group A has one 8-bit bidirectional data port and five control and status bits from port C. You can use port A and port B in two different modes. Modes 1 and 2 use handshaking signals from port C to synchronize data transfers. Refer to Chapter 4, *Theory of Operation*, or to Appendix B, *OKI 82C55A Data Sheet,* for more detailed information.

Digital I/O Connector

All digital I/O is transmitted through a standard, 50-pin, male connector. Pin 49 is connected to +5 V through a resettable protection fuse. You can use this +5 V supply to operate I/O module mounting racks. Even-numbered pins are connected to ground. See the *Optional Equipment* section in Chapter 1, *Introduction*, as well as Chapter 3, *Signal Connections*, for additional information.

Appendix A

Specifications

This appendix lists the specifications for the PC-DIO-24/PnP board. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° to 70° C.

Digital I/O

Number of channels .....24 I/O

Compatibility .....TTL

Absolute max voltage input rating (Vcc = 5.0 V) .....–0.5 to +5.5 V with respect to GND

Handshaking .....Requires one port

Power-on state .....Configured as inputs, pulled high or low (jumper-selectable)

Data transfers .....Interrupts, programmed I/O

Digital Logic Levels

Input Signals

The maximum input logic high and output logic high voltages assume a Vcc supply voltage of 5.0 V.

Level	Min	Max
Input logic high voltage	2.2 V	5.3 V
Input logic low voltage	–0.3 V	0.8 V
Input high current (V_{in} = 5 V, W1 set to pullup)	—	11.0 µA

Level	Min	Max
Input high current (V_{in} = 5 V, W1 set to pulldown)	—	65 µA
Input logic low current (V_{in} = 0 V, W1 set to pullup)	—	–65 µA
Input logic low current (V_{in} = 0 V, W1 set to pulldown)	—	–11 µA

Output Signals

Pin 49 (at 4.65 to 5.25 VDC)..... 1.0 A max

Level	Min	Max
Output logic high voltage (I_{ol} = –2.5 mA)	3.7 V	5.0 V
Output logic high voltage (I_{oh} = –4 mA)	2.7 V	5.0 V
Output logic low voltage (I_{ol} = 2.5 mA)	0 V	0.4 V
Output logic low voltage (I_{ol} = 4 mA)	0 V	0.5 V

Power Requirement

+5 VDC (±10%)..... 0.45 A typ, 1 A max

Physical

Dimensions ..... 11.7 by 10.6 cm (4.6 by 4.2 in.)

I/O connector ..... 50-pin male ribbon-cable connector

Environment

Operating temperature .....0° to 70° C

Storage temperature .....–55° to 150° C

Relative humidity .....5% to 90% noncondensing

Transfer Rates

Max with NI-DAQ software.....50 kbytes/s

Constant sustainable rate (typ).....1 to 10 kbytes/s

Transfer rates are a function of the speed with which your program reads data from or writes data to the board, and therefore vary with your system, software, and application. The following primary factors control PC-DIO-24/PnP transfer rates:

- Computer system performance
- Programming environment (register-level programming or NI-DAQ)
- Programming language and code efficiency
- Execution mode (foreground or background, with background execution typically using interrupts)
- Other operations in progress
- Application

For example, you can obtain higher transfer rates in a handshaking or data-transfer application, requiring an average rate, than in a pattern generation, data acquisition, or waveform generation application, requiring a constant sustainable rate.

The maximum rate shown was obtained using a 233 MHz Pentium computer running NI-DAQ and LabWindows/CVI software, with interrupt-based execution, and with no other high-speed operations in progress.

OKI 82C55A Data Sheet

Appendix
B

This appendix contains the manufacturer data sheet for the OKI Semiconductor* 82C55A CMOS PPI. This interface is used on the PC-DIO-24/PnP board.

OKI Semiconductor Data Book *Microprocessor*, Eighth Edition, January 1995.

OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

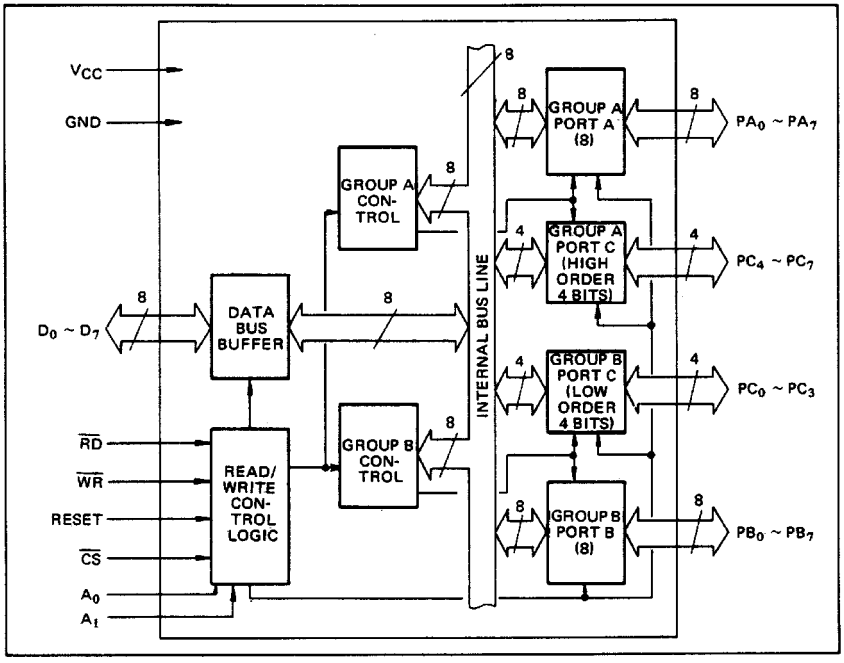
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

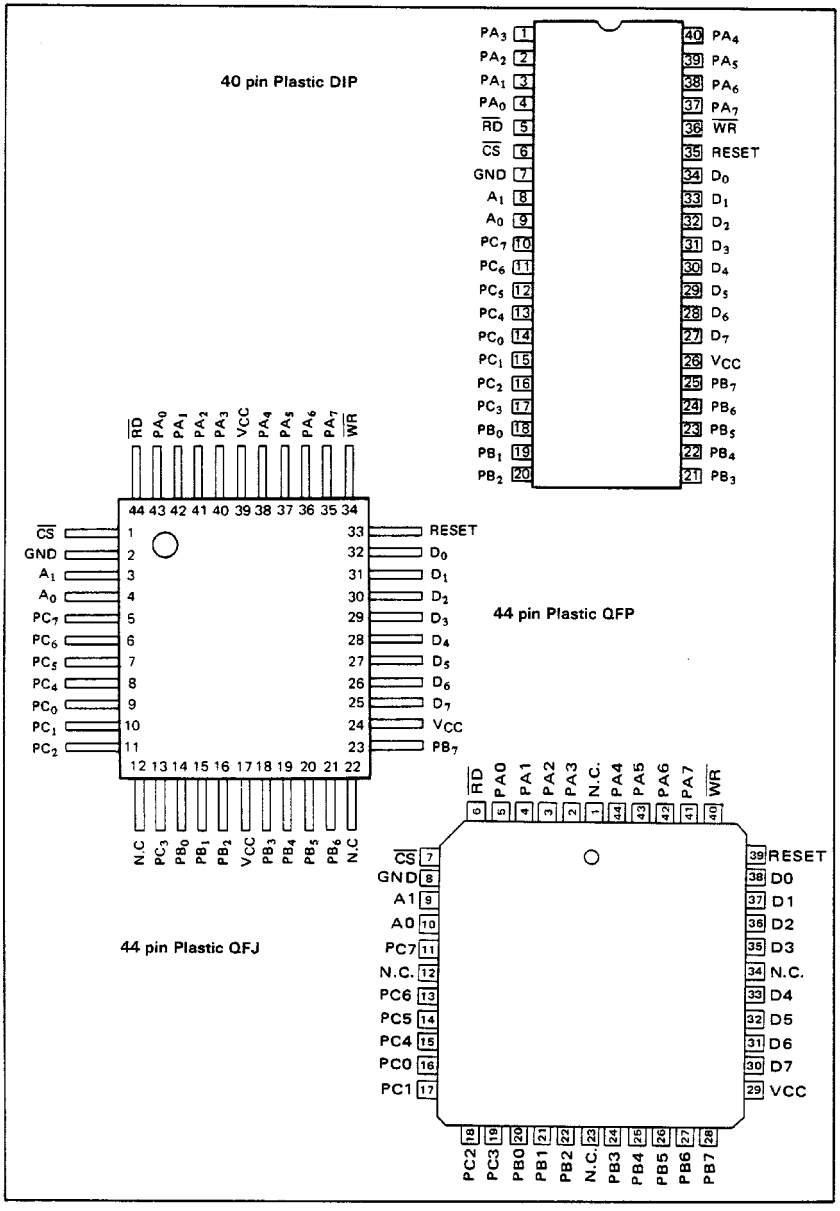
FEATURES

- High speed and low power consumption due to 3μ silicon gate CMOS technology
- 3V to 6V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600): MSM82C55A-2RS
- 44 pin Plastic QFJ (QFJ44-P-S650): MSM82C55A-2JS
- 44 pin Plastic QFP (QFP44-P-910-2K): MSM82C55A-2GS-2K

CIRCUIT CONFIGURATION



PIN CONFIGURATION (Top View)



■ I/O-MSM82C55A-2RS/GS/VJS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	−	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2			Unit
				Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA		4.2			V
		I_{OH} = −2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geqq V_{CC}$ −0.2V $V_{IH} \geqq V_{CC}$ −0.2V $V_{IL} \leqq$ 0.2V			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O write cycle 82C55A-2 ... 8MHzCPU timing				8	mA

AC CHARACTERISTICS

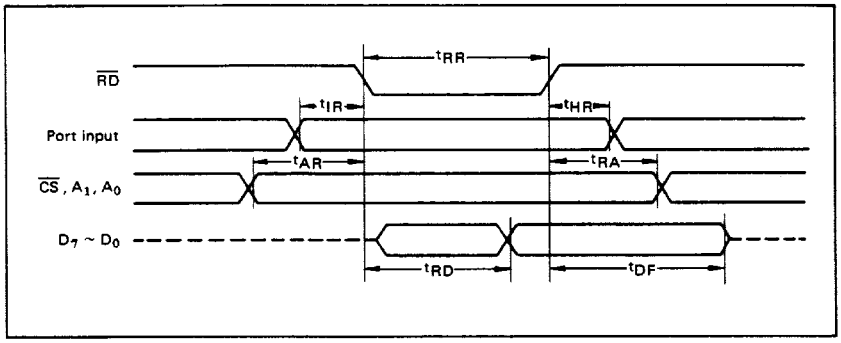
(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	Load 150 pF
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

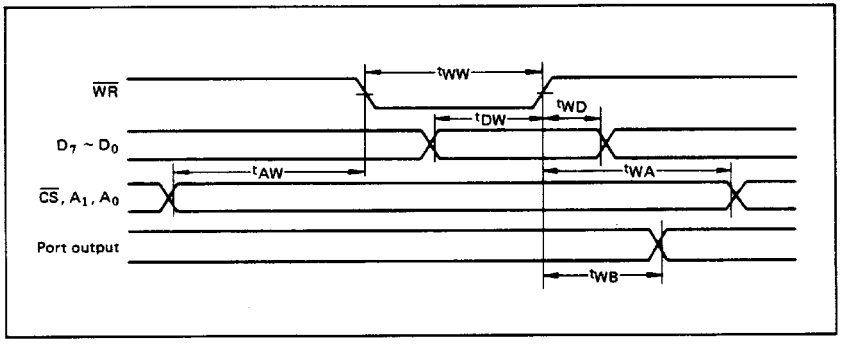
Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

■ I/O-MSM82C55A-2RS/GS/VJS ■

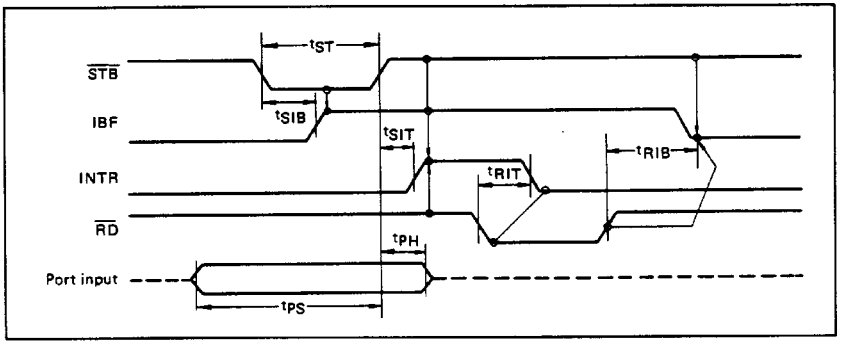
Basic Input Operation (Mode 0)



Basic Output Operation (Mode 0)



Strobe Input Operation (Mode 1)



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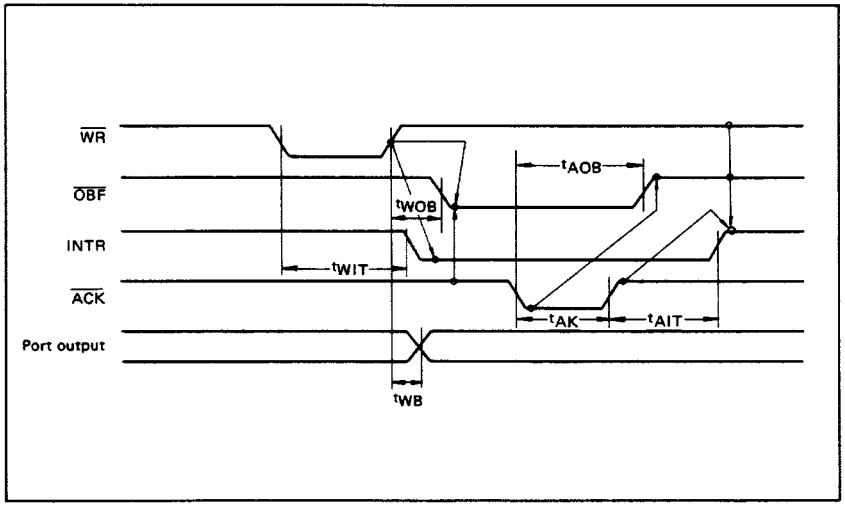
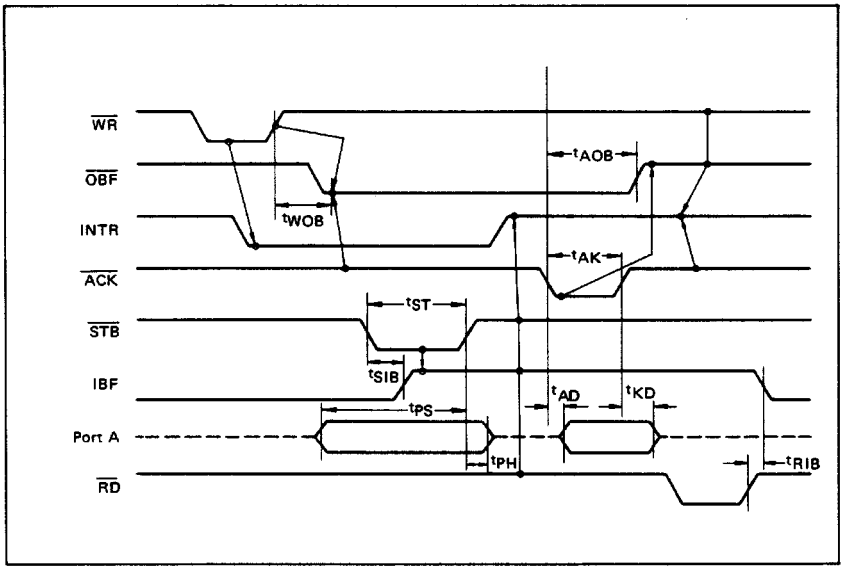
Strobe Output Operation (Mode 1)



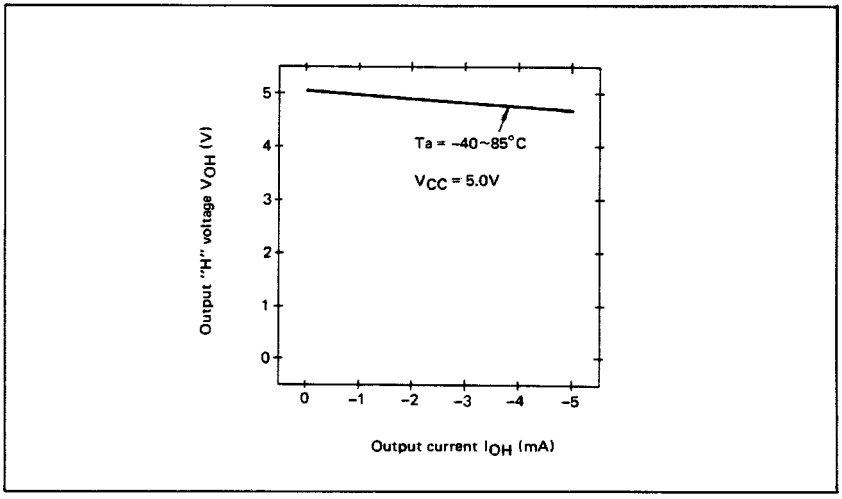
Bidirectional Bus Operation (Mode 2)



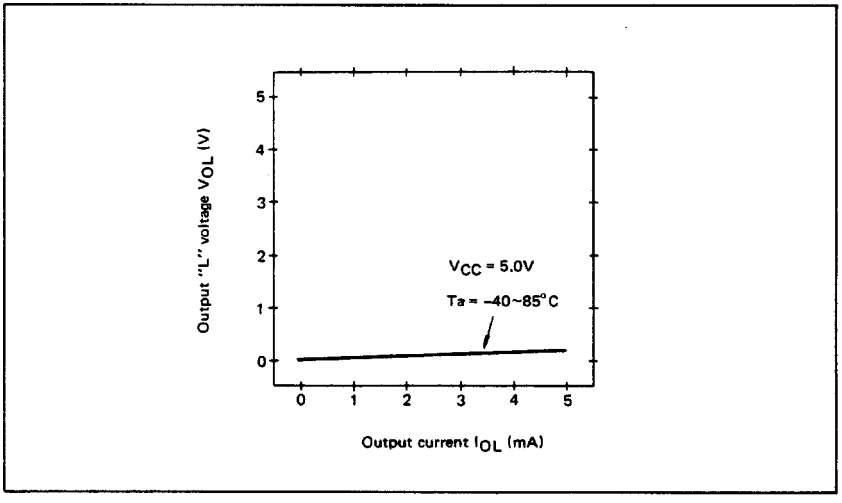
■ I/O-MSM82C55A-2RS/GS/VJS ■

OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

■ I/O-MSM82C55A-2RS/GS/VJS ■

FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to 0. and all ports groups are set to mode 0.
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
V_{CC}			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

■ I/O-MSM82C55A-2RS/GS/VJS ■

OPERATIONAL DESCRIPTION

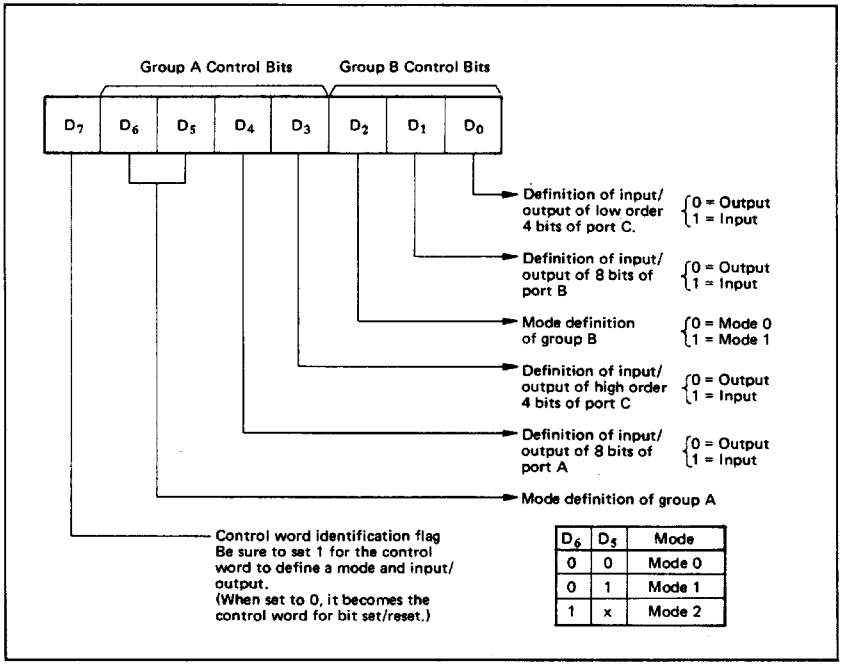
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



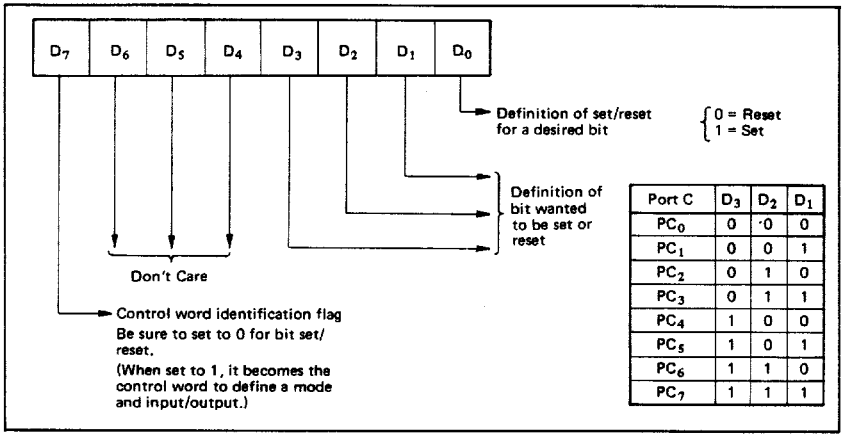
D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.



Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

■ I/O-MSM82C55A-2RS/GS/VJS ■

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

  $INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

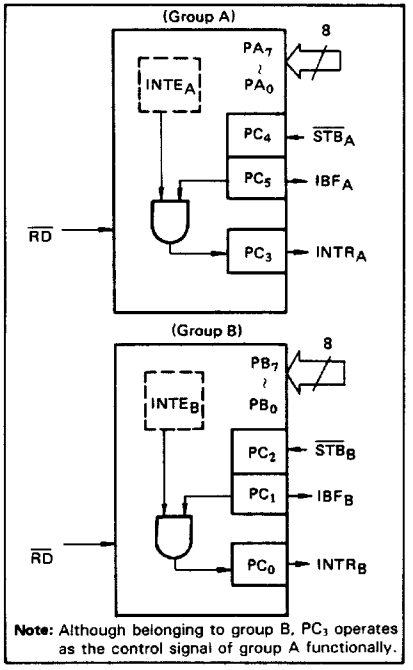
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

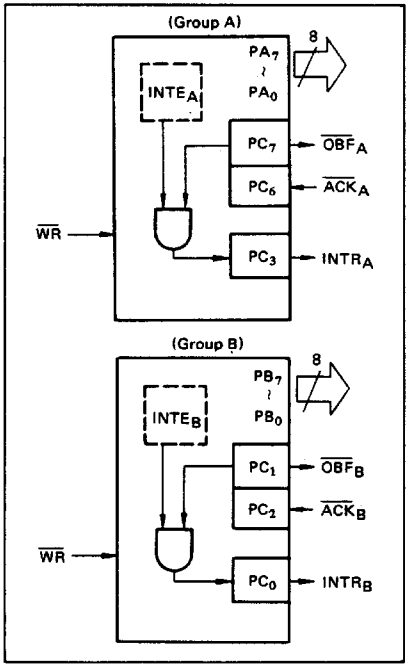
  $INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output

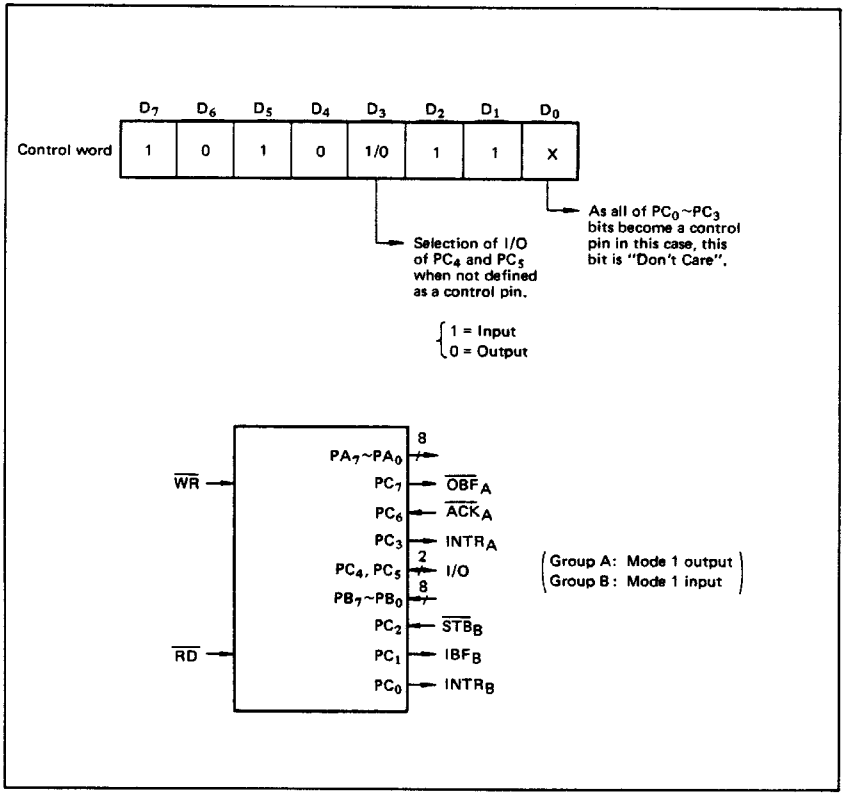


Port C Function Allocation in Mode 1

Combination of Input/Output / Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.



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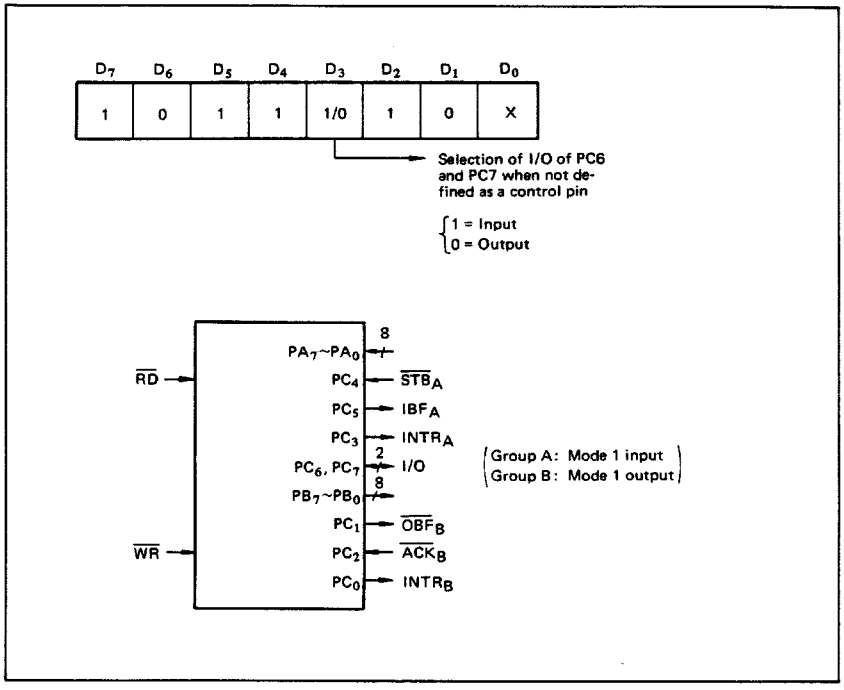
(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

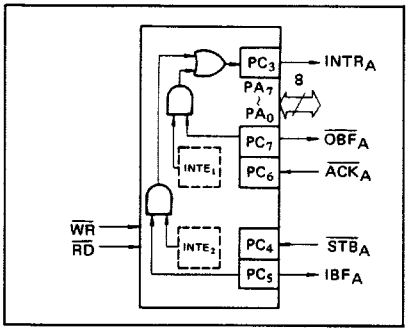
IBF (Input buffer full flag output)

- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

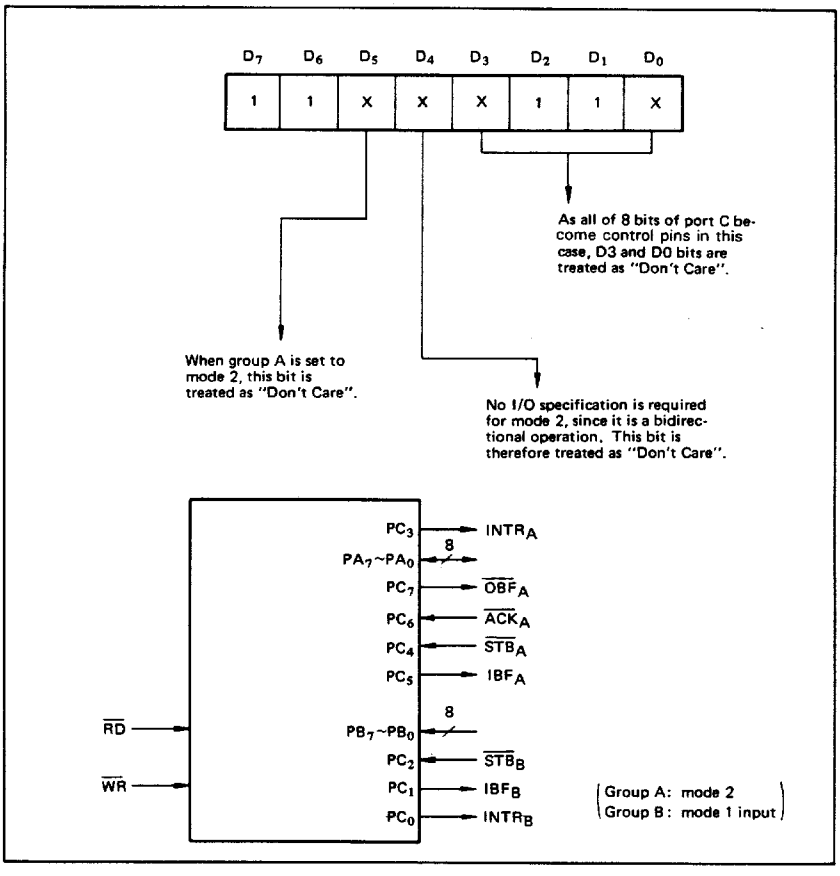
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



■ I/O-MSM82C55A-2RS/GS/VJS ■

4. When Group A is Different in Mode from Group B
Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.
The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note: Comparison of MSM82C55A-5 and MSM82C55A-2

MSM82C55A-5

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

MSM82C55A-2

After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC). 00H is ontput at the beginning of a write command when the output port is assigned.

Register-Level Programming

Appendix C

This appendix describes in detail the address and function of each of the PC-DIO-24/PnP control and status registers. This appendix also includes important information about register-level programming on the PC-DIO-24/PnP along with program examples written in C and assembly language.

☞ **Note:** ***If you plan to do application-level programming using software such as LabVIEW, LabWindows/CVI, or NI-DAQ with your PC-DIO-24/PnP board, you need not read this appendix.***

Introduction

You can configure your PC-DIO-24PnP board to use base addresses in the range of 100 to 3E0 hex. Your PC-DIO-24PnP board occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140..., 3E0 hex. The base I/O address is software-configured and does not require you to manually change any board settings. For more information on configuring the PC-DIO-24PnP, see Chapter 2, *Installation and Configuration*.

The PC-DIO-24 non-PnP board occupies four bytes of address space and must be located on a four-byte boundary. For more information on configuring the PC-DIO-24, see Appendix D, *Using Your PC-DIO-24 (Non-PnP) Board*.

In addition to the 82C55A device, the PC-DIO-24PnP has two registers that select which interrupt sources are capable of generating interrupts. Individual enable bits select whether port A or port B interrupt signals from the 82C55A device generate interrupt requests. A master interrupt enable bit determines whether the board can actually send interrupt requests to the host computer. The configuration bits for these registers are defined in the *Register Description for the Interrupt Control Registers* section in this appendix.

The PC-DIO-24 (non-PnP) does not have interrupt control registers. Instead, it uses one of the port C lines to enable or disable interrupts. See Appendix D, *Using Your PC-DIO-24 (Non-PnP) Board* for more information.

The three 8-bit ports of the 82C55A are divided into two groups of 12 signals each: group A and group B. One 8-bit control word selects the modes of operation for both groups. The group A control bits configure port A (A7 through A0) and the upper 4 bits (nibble) of port C (C7 through C4). The group B control bits configure port B (B7 through B0) and the lower nibble of port C (C3 through C0). These configuration bits are defined in the *Register Description for the 82C55A* section later in this appendix.

The 82C55A potentially requires up to 200 ns recovery time between consecutive read or write cycles. Certain computers may provide slightly less time than this between two back-to-back assembly-language reads or writes. If you are programming in assembly language, it is therefore recommended that you separate two 82C55A reads or writes with at least one other instruction.

Register Map

The following table lists the address map for the PC-DIO-24/PnP.

Table C-1. PC-DIO-24/PnP Address Map

Register Name	Offset Address (Hex)	Size	Type
82C55A Register Group			
PORTA Register	00	8-bit	Read-and-write
PORTB Register	01	8-bit	Read-and-write
PORTC Register	02	8-bit	Read-and-write
CNFG Register	03	8-bit	Write-only
Interrupt Control Register Group (PC-DIO-24PnP only)			
Register 1	14	8-bit	Write-only
Register 2	15	8-bit	Write-only

Register Description for the 82C55A

Figure C-1 shows the two control word formats used to completely program the 82C55A. The control word flag determines which control word format is being programmed. When the control word flag is 1, bits 6 through 0 select the I/O characteristics of the 82C55A ports. These bits also select the mode in which the ports are operating (that is, mode 0, mode 1, or mode 2). When the control word flag is 0, bits 3 through 0 select the bit set/reset format of port C.

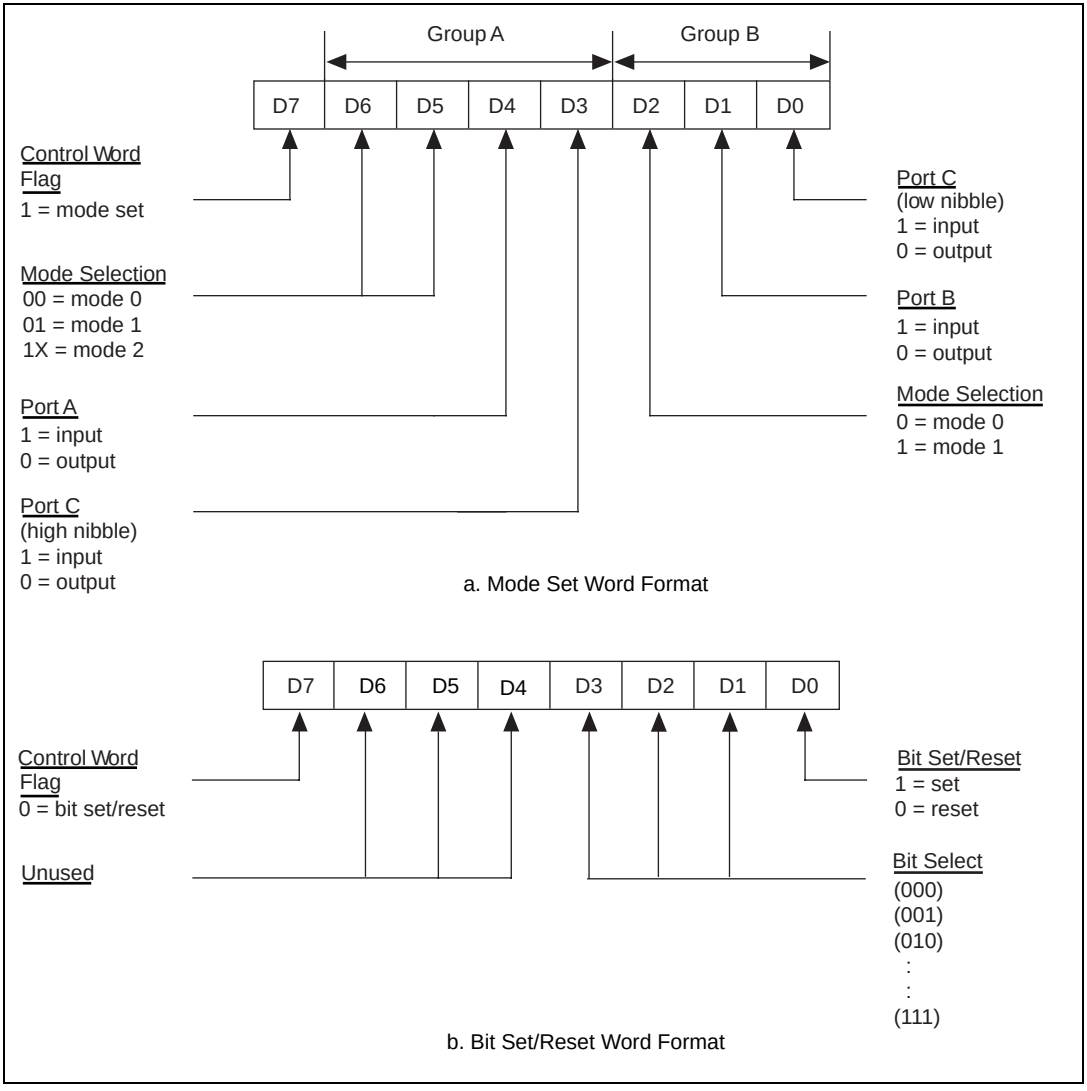


Figure C-1. Control Word Formats for the 82C55A

Caution: ***During programming, note that each time any port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table C-2 shows the control words for setting or resetting each bit in port C. Notice that bit 7 of the control word is cleared when programming the set/reset option for the bits of port C.

Table C-2. Port C Set/Reset Control Words

Bit Number	Bit Set Control Word	Bit Reset Control Word	The Bit Set or Reset in Port C
0	0xxx0001	0xxx0000	xxxxxxxb
1	0xxx0011	0xxx0010	xxxxxxbx
2	0xxx0101	0xxx0100	xxxxxbxx
3	0xxx0111	0xxx0110	xxxxbxxx
4	0xxx1001	0xxx1000	xxxbxxxx
5	0xxx1011	0xxx1010	xxbxxxxx
6	0xxx1101	0xxx1100	xbxxxxxx
7	0xxx1111	0xxx1110	bxxxxxxx

Register Description for the Interrupt Control Registers

There are two interrupt control registers on the PC-DIO-24PnP. One of these registers has individual enable bits for the two interrupt lines from the 82C55A device. The other register has a master interrupt enable bit. When writing to these registers, set all reserved bits to zero. The bit maps and signal definitions are listed as follows.

Interrupt Control Register 1 (PnP Board Only)

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	IRQ1	IRQ0

Bit	Name	Description
2–7	x	Reserved bit.
1	IRQ1	PPI Interrupt Request for Port B—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, the PPI can send an interrupt, INTRB, to the host computer. If this bit is cleared, the PPI does not send the interrupt INTRB to the host computer, regardless of the setting of INTEN.
0	IRQ0	PPI Interrupt Request for Port A—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, the PPI can send an interrupt, INTRA, to the host computer. If this bit is cleared, the PPI does not send the interrupt INTRA to the host computer, regardless of the setting of INTEN.

Interrupt Control Register 2 (PnP Board Only)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	INTEN	X	X

Bit	Name	Description
1–0, 3–7	X	Reserved Bit.
2	INTEN	Global Interrupt Enable Bit—If this bit is set, the PC-DIO-24PnP can interrupt the host computer. If this bit is cleared, the board cannot interrupt the host computer.

Programming Considerations for the 82C55A

Modes of Operation for the 82C55A

The three basic modes of operation for the 82C55A are as follows:

- Mode 0—Basic I/O
- Mode 1—Strobed I/O
- Mode 2—Bidirectional bus

The 82C55A also has a single bit set/reset feature for port C, which is programmed by the 8-bit control word. For additional information, refer to Appendix B, *OKI 82C55A Data Sheet*.

Mode 0

Use this mode for simple input and output operations for each of the ports. No handshaking is required; simply write data to or read data from a specified port.

Mode 0 has the following features:

- Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibbles of port C).
- Any port can be input or output.
- Outputs are latched, but inputs are not latched.

Mode 1

This mode transfers data that is synchronized by handshaking signals. Ports A and B use the eight lines of port C to generate or receive the handshake signals. This mode divides the ports into two groups (group A and group B) and includes the following features:

- Each group contains one 8-bit data port (port A or port B) and one 3-bit control/status port (upper or lower portion of port C).
- The 8-bit data ports can be either input or output, both of which are latched.
- The 3-bit ports are used for control and status of the 8-bit data ports.
- Interrupt generation and enable/disable functions are available.

Mode 2

Use this mode for communication over a bidirectional 8-bit bus. Handshaking signals are used in a manner similar to mode 1. Mode 2 is available for use in group A only (port A and the upper portion of port C). Other features of this mode include the following:

- One 8-bit bidirectional port (port A) and a 5-bit control/status port (port C).
- Latched inputs and outputs.
- Interrupt generation and enable/disable functions.

Single Bit Set/Reset Feature

You can set or reset any of the eight bits of port C with one control word. This feature generates control signals for port A and port B when these ports are operating in mode 1 or mode 2.

Mode 0—Basic I/O

Use mode 0 for simple I/O functions (no handshaking) for each of the three ports. You can assign each port as an input or an output port. The 16 possible I/O configurations are shown in Table C-3. Notice that bit 7 of the control word is set when programming the mode of operation for each port.

Table C-3. Mode 0 I/O Configurations

Number	Control Word	Group A		Group B	
	Bit 76543210	Port A	Port C[1]	Port B	Port C[2]
0	10000000	Output	Output	Output	Output
1	10000001	Output	Output	Output	Input
2	10000010	Output	Output	Input	Output
3	10000011	Output	Output	Input	Input
4	10001000	Output	Input	Output	Output
5	10001001	Output	Input	Output	Input
6	10001010	Output	Input	Input	Output
7	10001011	Output	Input	Input	Input
8	10010000	Input	Output	Output	Output

Table C-3. Mode 0 I/O Configurations (Continued)

Number	Control Word	Group A		Group B	
	Bit 76543210	Port A	Port C[1]	Port B	Port C[2]
9	10010001	Input	Output	Output	Input
10	10010010	Input	Output	Input	Output
11	10010011	Input	Output	Input	Input
12	10011000	Input	Input	Output	Output
13	10011001	Input	Input	Output	Input
14	10011010	Input	Input	Input	Output
15	10011011	Input	Input	Input	Input

[1] Upper nibble of port C
[2] Lower nibble of port C

Mode 0 Programming Example

The following example shows how to configure the 82C55A for various combinations of mode 0 input and output. This code is strictly an example and is not intended to be used without modification in a practical situation.

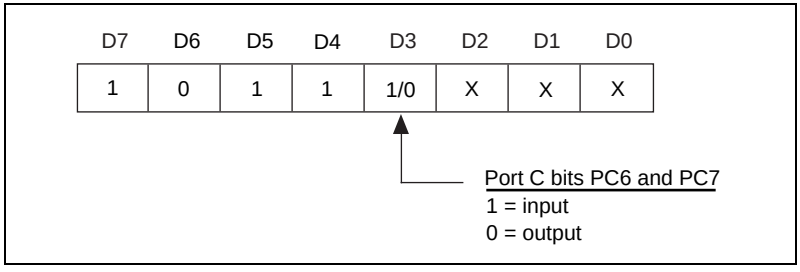
```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define PORTAoffset        0x00         /* Offset for port A */
#define PORTBoffset        0x01         /* Offset for port B */
#define PORTCoffset        0x02         /* Offset for port C */
#define CNFGoffset         0x03         /* Offset for CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */
porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1*/

outp(cnfg,0x80);           /* Ports A, B, and C are outputs. */
outp(porta,0x12);          /* Write data to port A. */
outp(portb,0x34);          /* Write data to port B. */
```

```
outp(portc,0x56);          /* Write data to port C. */

/* EXAMPLE 2*/

outp(cnfg,0x90);           /* Port A is input; ports B and C are outputs. */
outp(portb,0x22);          /* Write data to port B. */
outp(portc,0x55);          /* Write data to port C. */
valread = inp(porta);      /* Read data from port A. */

/* EXAMPLE 3 */

outp(cnfg,0x82);           /* Ports A and C are outputs;
                              port B is an input. */

/* EXAMPLE 4 */

outp(cnfg,0x89);           /* Ports A and B are outputs;
                              port C is an input. */
}
```

Mode 1—Strobed Input

In mode 1, the digital I/O bits are divided into two groups: group A and group B. Each of these groups contains one 8-bit port and one 3-bit control/data port. The 8-bit port can be either an input or an output port, and the 3-bit port is used for control and status information for the 8-bit port. The transfer of data is synchronized by handshaking signals in the 3-bit port.

The control word written to the CNFG Register to configure port A for input in mode 1 is shown as follows. Use bits PC6 and PC7 of port C as extra input or output lines.



The control word written to the CNFG Register to configure port B for input in mode 1 is shown as follows. Notice that port B does not have extra input or output lines left from port C when ports A and B are both enabled for handshaking.

D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	X	1	1	X

During a mode 1 data read transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for an input transfer are shown as follows.

Port C status-word bit definitions for input (port A and port B):

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7–6	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 input. If these bits are configured for output, the port C bit set/reset function must be used to manipulate them.
5	IBFA	Input Buffer for Port A—A high setting indicates that data has been loaded into the input latch for port A.
4	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—When INTEA and IBFA are high, this bit is high, indicating that an interrupt request is pending for port A.
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables interrupts from port B of the 82C55A. This bit is controlled by setting/resetting PC2.
1	IBFB	Input Buffer for Port B—A high setting indicates that data has been loaded into the input latch for port B.

0	INTRB	Interrupt Request Status for Port B—When INTEB and IBFB are high, this bit is high, indicating that an interrupt request is pending for port B.

At the digital I/O connector, port C has the following pin assignments when in mode 1 input. Notice that the status of STBA* and the status of STBB* are not included in the port C status word.

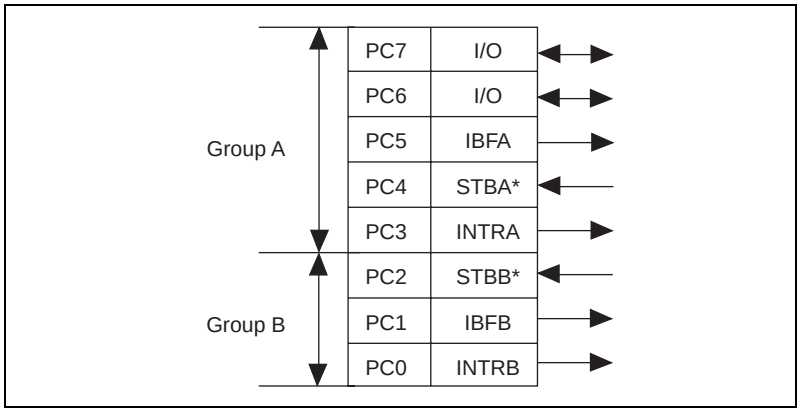


Figure C-2. Port C Pin Assignments, Mode 1 Input

Mode 1 Input Programming Example

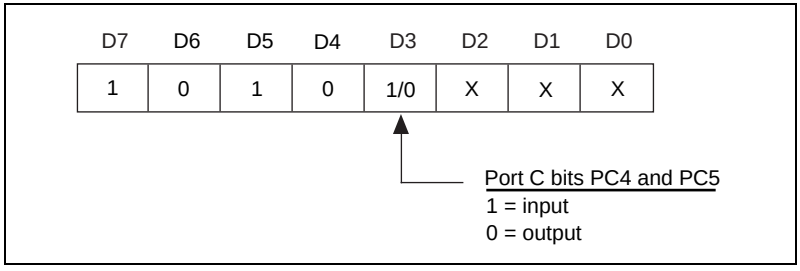
The following example shows how to configure PPI A for various combinations of mode 1 input. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define PORTAoffset        0x00         /* Offset for port A */
#define PORTBoffset        0x01         /* Offset for port B */
#define PORTCoffset        0x02         /* Offset for port C */
#define CNFGoffset         0x03         /* Offset for CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;
```

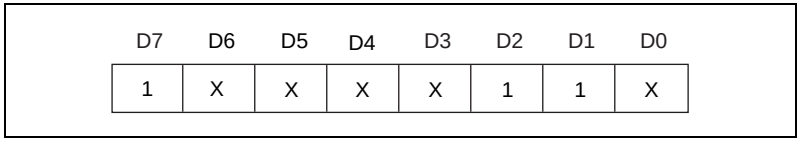
```
/* EXAMPLE 1–port A input */
outp(cnfg,0xB0);                        /* Port A is an input in mode 1. */
while (!(inp(portc) & 0x20));           /* Wait until IBFA is set,
                                           indicating that data has been
                                           loaded in port A. */
valread = inp(porta);                   /* Read the data from port A. */
/* EXAMPLE 2–Port B input */
outp(cnfg,0x86);                        /* Port B is an input in mode 1. */
while (!(inp(portc) & 0x02));           /* Wait until IBFB is set,
                                           indicating that data has been
                                           loaded in port B. */
valread = inp(portb);
}
```

Mode 1—Strobed Output

The control word written to the CNFG Register to configure port A for output in mode 1 is shown as follows. Bits PC4 and PC5 of port C can be used as extra input or output lines.



The control word written to the CNFG Register to configure port B for output in mode 1 is shown as follows. Notice that port B does not have extra input or output lines left from port C when ports A and B are both enabled for handshaking.



During a mode 1 data write transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. Notice that the bit definitions are different for a write and a read transfer.

Port C status-word bit definitions for output (port A and port B):

D7	D6	D5	D4	D3	D2	D1	D0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB	OBFB*	INTRB

Bit	Name	Description
7	OBFA*	Output Buffer for Port A—A low setting indicates that the CPU has written data to port A.
6	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC6.
5–4	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 output. If these bits are configured for output, the port C bit set/reset function must be used to manipulate them.
3	INTRA	Interrupt Request Status for Port A—When INTEA and OBFA* are high, this bit is high, indicating that an interrupt request is pending for port A.
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables interrupts from port B of the 82C55A. This bit is controlled by setting/resetting PC2.
1	OBFB*	Output Buffer for Port B—A low setting indicates that the CPU has written data to port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB and OBFB* are high, this bit is high, indicating that an interrupt request is pending for port B.

At the digital I/O connector, port C has the following pin assignments when in mode 1 output. Notice that the status of ACKA* and the status of ACKB* are not included when port C is read.

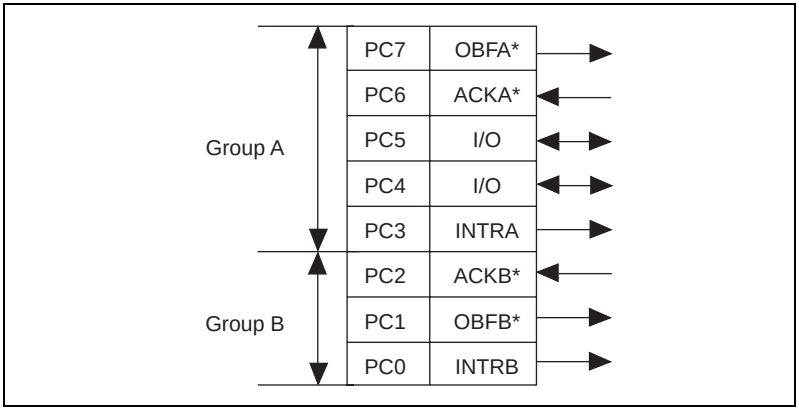


Figure C-3. Port C Pin Assignments, Mode 1 Output

Mode 1 Output Programming Example

The following example shows how to configure PPI A for various combinations of mode 1 output. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define PORTAoffset        0x00         /* Offset for port A */
#define PORTBoffset        0x01         /* Offset for port B */
#define PORTCoffset        0x02         /* Offset for port C */
#define CNFGoffset         0x03         /* Offset for CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;

/* EXAMPLE 1–port A output */

outp(cnfg,0xA0);                       /* Port A is an output in mode 1.*/
while (!(inp(portc) & 0x80));          /* Wait until OBFA* is set,
                                          indicating that the data last
                                          written to port A has been
                                          read.*/
outp(porta,0x12);                      /* Write data to port A. */
```

```
/* EXAMPLE 2–port B output */
outp(cnfg,0x84);                        /* Port B is an output in mode 1.*/
while (!(inp(portc) & 0x02));           /* Wait until OBFB* is set,
                                           indicating that the data last
                                           written to port B has been
                                           read.*/
outp(portb,0x34);                       /* Write the data to port B. */
}
```

Mode 2—Bidirectional Bus

Mode 2 has an 8-bit bus that can transfer both input and output data without changing the configuration. The data transfers are synchronized with handshaking lines in port C. This mode uses only port A; however, port B can be used in either mode 0 or mode 1 while port A is configured for mode 2.

The control word written to the CNFG Register to configure port A as a bidirectional data bus in mode 2 is shown as follows. If port B is configured for mode 0, then PC2, PC1, and PC0 of port C can be used as extra input or output lines.

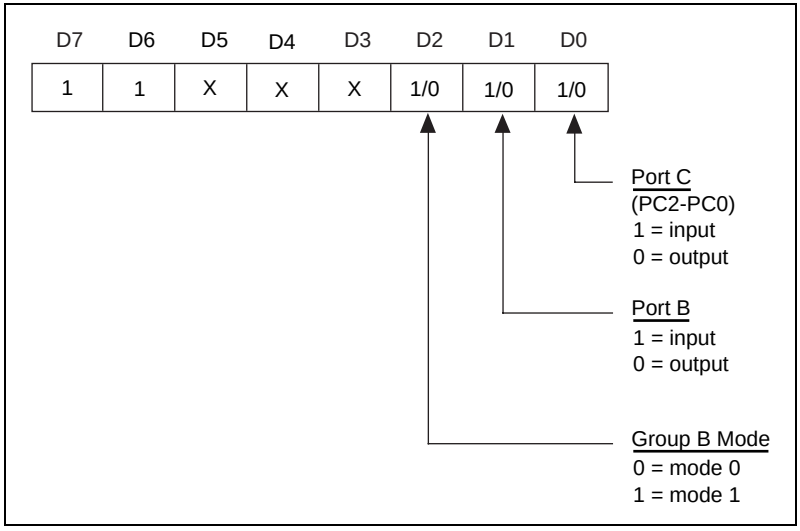


Figure C-4. Port A Configured as a Bidirectional Data Bus in Mode 2

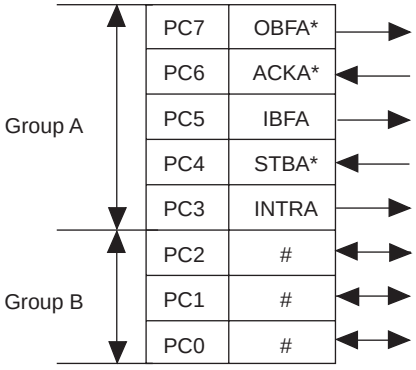
During a mode 2 data transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for a mode 2 transfer are shown as follows.

Port C status-word bit definitions for bidirectional data path (port A only):

D7	D6	D5	D4	D3	D2	D1	D0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output Buffer for Port A—A low setting indicates that the CPU has written data to port A.
6	INTE1	Interrupt Enable Bit for Port A Output Interrupts—Setting this bit enables output interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC6.
5	IBFA	Input Buffer for Port A—A high setting indicates that data has been loaded into the input latch of port A.
4	INTE2	Interrupt Enable Bit for Port A Input Interrupts—Setting this bit enables input interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—If INTE1 and IBFA are high, then this bit is high, indicating that an interrupt request is pending for port A input transfers. If INTE2 and OBFA* are high, then this bit is high, indicating that an interrupt request is pending for port A output transfers.
2–0	I/O	Input/Output—These bits can be used for general-purpose I/O lines if group B is configured for mode 0. If group B is configured for mode 1, refer to the bit explanations shown in the preceding mode 1 sections.

At the digital I/O connector, port C has the following pin assignments when in mode 2. Notice that the status of STBA* and the status of ACKA* are not included in the port C status word.



\# The three port C lines associated with group B function are based on the mode selected for group B; that is, if group B is configured for mode 0, PC2-PC0 function as general-purpose input/output, but if group B is configured for mode 1 input or output, PC2-PC0 function as handshaking lines as shown in the preceding mode 1 sections.

Figure C-5. Port C Pin Assignments, Mode 2

Mode 2 Programming Example

The following example shows how to configure PPI A for mode 2 input and output and how to use the handshaking signals to control data flow. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define PORTAoffset        0x00         /* Offset for port A */
#define PORTBoffset        0x01         /* Offset for port B */
#define PORTCoffset        0x02         /* Offset for port C */
#define CNFGoffset         0x03         /* Offset for CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
```

```
cnfg  = BASE_ADDRESS + CNFGoffset;
/* EXAMPLE 1*/
outp(cnfg,0xC0);                        /* Port A is in mode 2. */
while (!(inp(portc) & 0x80));           /* Wait until OBFA* is set,
                                           indicating that the data last
                                           written to port A has been read.
                                           */
outp(porta,0x67);                       /* Write the data to port A. */
while (!(inp(portc) & 0x20));           /* Wait until IBFA is set,
                                           indicating that data is
                                           available in port A to be read.
                                           */
valread = inp(porta);                   /* Read data from port A. */
}
```

Interrupt Programming Examples for the 82C55A

The following examples show the process required to enable interrupts for several different operating modes. The interrupt handling routines and interrupt installation routines for the 82C55A are not included. Consult your computer technical reference manual for additional information. Also, if you generate interrupts with the PC3 or PC0 lines of the 82C55A devices, you must maintain the active high level until the interrupt service routine is entered. Otherwise, the host computer considers the interrupt a spurious interrupt and routes the request to the channel responsible for handling spurious interrupts. To prevent this problem, try using some other I/O bit to send feedback to the device generating the interrupt. In this way, the interrupting device can be signaled that the interrupt service routine has been entered. For further information on using PC3 and PC0 for interrupts, see the *Interrupt Handling* section later in this appendix.

☞ **Note:** ***The following code applies to the PC-DIO-24PnP. To adapt this code to the PC-DIO-24 (non-PnP), remove the*** `outp (ireg1)` ***instructions and replace*** `outp (ireg2, 0x04)` ***with the following (assuming you use PC4 as your interrupt enable):***

```
outp (cnfg, 0x08) /* Clear PC4 to enable interrupts */
```

You cannot use PC4 as your interrupt enable in examples 1, 5, or 6, because these configurations use PC4 for handshaking.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define PORTAoffset        0x00         /* Offset for port A */
#define PORTBoffset        0x01         /* Offset for port B */
#define PORTCoffset        0x02         /* Offset for port C */
#define CNFGoffset         0x03         /* Offset for CNFG */
#define IREG1offset        0x14         /* Offset for Interrupt Reg. 1 */
#define IREG2offset        0x15         /* Offset for Interrupt Reg. 2 */

unsigned int porta, portb, portc, cnfg, ireg1, ireg2;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + PORTAoffset;
portb = BASE_ADDRESS + PORTBoffset;
portc = BASE_ADDRESS + PORTCoffset;
cnfg  = BASE_ADDRESS + CNFGoffset;
ireg1 = BASE_ADDRESS + IREG1offset;
ireg2 = BASE_ADDRESS + IREG2offset;

/* EXAMPLE 1–Set up interrupts for mode 1 input for port A. Enable the
   appropriate interrupt bits. */

outp(cnfg,0xB0);           /* Port A is an input in mode 1. */
outp(cnfg,0x09);           /* Set PC4 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set IRQ0 to enable port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 2–Set up interrupts for mode 1 input for port B. Enable the
   appropriate interrupt bits. */

outp(cnfg,0x86);           /* Port B is an input in mode 1. */
outp(cnfg,0x05);           /* Set PC2 to enable interrupts from 82C55A. */
outp(ireg1,0x02);          /* Set IRQ1 to enable port B interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 3–Set up interrupts for mode 1 output for port A. Enable the
   appropriate interrupt bits. */

outp(cnfg,0xA0);           /* Port A is an output in mode 1. */
outp(cnfg,0x0D);           /* Set PC6 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set IRQ0 to enable port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 4–Set up interrupts for mode 1 output for port B. Enable the
                              appropriate interrupt bits. */

outp(cnfg,0x84);           /* Port B is an output in mode 1. */
outp(cnfg,0x05);           /* Set PC2 to enable interrupts from 82C55A. */
```

```
outp(ireg1,0x02);          /* Set IRQ1 to enable port B interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 5–Set up interrupts for mode 2 output transfers. Enable the
                              appropriate interrupt bits. */

outp(cnfg,0xC0);           /* Mode 2 output. */
outp(cnfg,0x0D);           /* Set PC6 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set IRQ0 to enable port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 6–Set up interrupts for mode 2 input transfers. Enable the
   appropriate interrupt bits. */

outp(cnfg,0xD0);           /* Mode 2 input. */
outp(cnfg,0x09);           /* Set PC4 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set IRQ0 to enable port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */
}
```

Interrupt Handling

☞ **Note:** ***This section applies only to the PC-DIO-24PnP. The PC-DIO-24 (non-PnP) does not implement the IRQ1, IRQ2, or INTEN bits. To enable and disable interrupts on the non-PnP board, see Appendix D,*** *Using Your PC-DIO-24 (Non-PnP) Board****.***

On the PC-DIO-24PnP, the INTEN bit of Interrupt Register 2 must be set to enable interrupts. This bit must first be cleared to disable unwanted interrupts. After all sources of interrupts have been disabled or placed in an inactive state, you can set INTEN.

To interrupt the host computer, program the selected 82C55A port for the I/O mode desired. In mode 1, set either the INTEA or the INTEB bit to enable interrupts from port A or port B, respectively. In mode 2, set either INTE1 or INTE2 for interrupts on output or input transfers, respectively. The INTE1 and INTE2 interrupt outputs are cascaded into a single interrupt output for port A. After enabling interrupts from the 82C55A, set the appropriate enable bit in Interrupt Control Register 1; for example, if you selected both mode 2 interrupts for port A, you would set IRQ0 in order to interrupt the host computer.

External signals can be used to interrupt the PC-DIO-24/PnP when port A or port B is in mode 0 and the low nibble of port C is configured for input. If port A is in mode 0, use PC3 to generate an interrupt; if

port B is in mode 0, use PC0 to generate an interrupt. Once you have configured the 82C55A, set the corresponding interrupt enable bit in Interrupt Control Register 1. If you are using PC3, set IRQ0; if you are using PC0, set IRQ1. When the external signal becomes logic high, an interrupt request occurs. Although the host computer's interrupt-monitoring circuitry is triggered by the positive-going edge of the interrupt signal, the signal must remain high until the interrupt routine has been entered and interrupts have been masked out. Make sure your external interrupt signal meets these qualifications. To disable the external interrupt, clear the appropriate IRQ bit or clear the INTEN bit.

Using Your PC-DIO-24 (Non-PnP) Board

Appendix D

This appendix describes the differences between the PC-DIO-24 and PC-DIO-24PnP boards, the PC-DIO-24 board configuration, and the PC-DIO-24 installation into your computer. Read this appendix only if you do *not* have the Plug and Play version of the board.

Differences between the PC-DIO-24PnP and the PC-DIO-24

The PC-DIO-24PnP is a Plug and Play upgrade from a legacy board, the PC-DIO-24. *Legacy board* refers to a board with switches and jumpers used to set the addresses and interrupt levels. The original legacy board was replaced with a backwards-compatible, revised PC-DIO-24 that has many of the new features of the Plug and Play version. The following list compares the specifications and functionality of the newer boards with the original legacy board. This document applies only to the revised PC-DIO-24/PnP board.

Table D-1. Comparison of Characteristics

Specification	Original PC-DIO-24	Revised PC-DIO-24	PC-DIO-24PnP
I/O base address selection	Uses switches	Uses switches	Plug and Play compatible
Interrupt request selection	Uses jumpers	Uses jumpers	Plug and Play compatible
Interrupt request enable	Uses one port C line (jumper selectable)	Uses one port C line (jumper selectable)	Software-controlled (uses interrupt control registers)

Table D-1. Comparison of Characteristics (Continued)

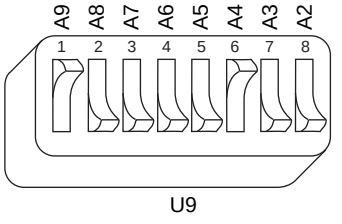
Specification	Original PC-DIO-24	Revised PC-DIO-24	PC-DIO-24PnP
5 V supply fuse	Nonresettable	Self-resetting	Self-resetting
Power-up state	No pullups or pulldowns	Jumper for pullup (factory default) or pulldown	Jumper for pullup (factory default) or pulldown

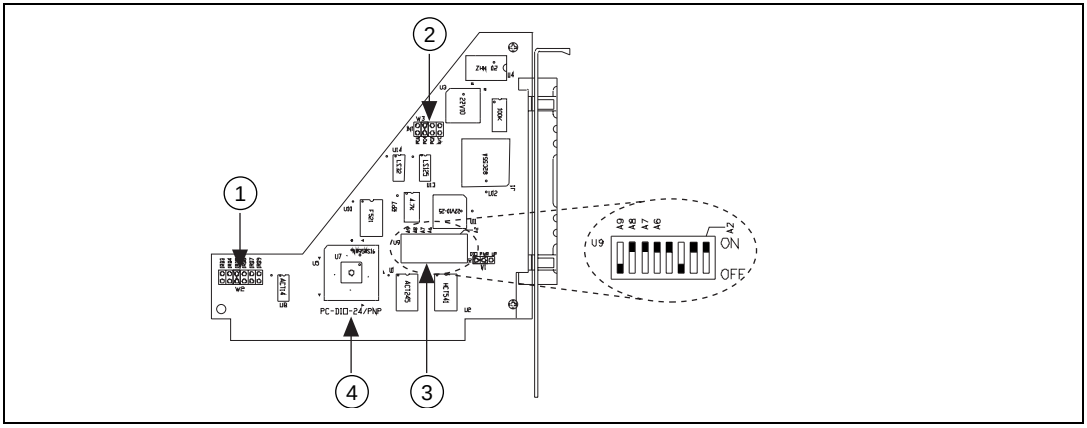
Configuration

The PC-DIO-24 contains one DIP switch and two jumpers to configure the base I/O address, interrupt level, and interrupt enable signal. Figure D-1 shows the location of DIP switch U9 and jumper sets W2 and W3.

The PC-DIO-24 is configured at the factory to a base I/O address of hex 210, to use interrupt enable line PC4, and to use interrupt level 5. These settings (shown in Table D-2) are suitable for most systems. However, if your system has other hardware at this base I/O address, interrupt enable line, or interrupt level, you need to change these settings on the PC-DIO-24 (as described in the following pages) or on the other hardware. Record your settings in the *PC-DIO-24/PnP Hardware and Software Configuration Form* in Appendix E, *Customer Communication*.

Table D-2. PC-DIO-24 Factory-Set Jumper and Switch Settings

Base I/O Address	Interrupt Enable Line	Interrupt Level
Hex 210 (factory setting)	PC4 (factory setting)	Interrupt level 5 selected (factory setting)
	W2: Row PC4	W3: IRQ5



1 W2	2 W3	3 U9	4 Product Name

Figure D-1. PC-DIO-24 Parts Locator Diagram

Base I/O Address Settings

The base I/O address for the PC-DIO-24 is determined by the switches at position U9 (see Figure 2-1). The switches are set at the factory for the I/O address hex 210. With this default setting, the PC-DIO-24 uses the I/O address space hex 210 through 213.

☞ **Note:** ***Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this I/O address space, you must change the base I/O address for the PC-DIO-24 or for the other device.***

Each switch in U9 corresponds to one of the address lines A9 through A2. For space reasons, not all address lines are separately labeled on the board. The range for possible base I/O address settings is hex 000 through 3FC. Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O values hex 100 through 3FF are available on the I/O channel. A1 and A0 are used by the PC-DIO-24 to decode the onboard registers. On the U9 DIP switches, press the side marked *OFF* to select a binary value of 1 for the corresponding address bit. Press the other side of the switch to select a binary value of 0 for the corresponding address bit. Figure D-2 shows two possible switch settings.

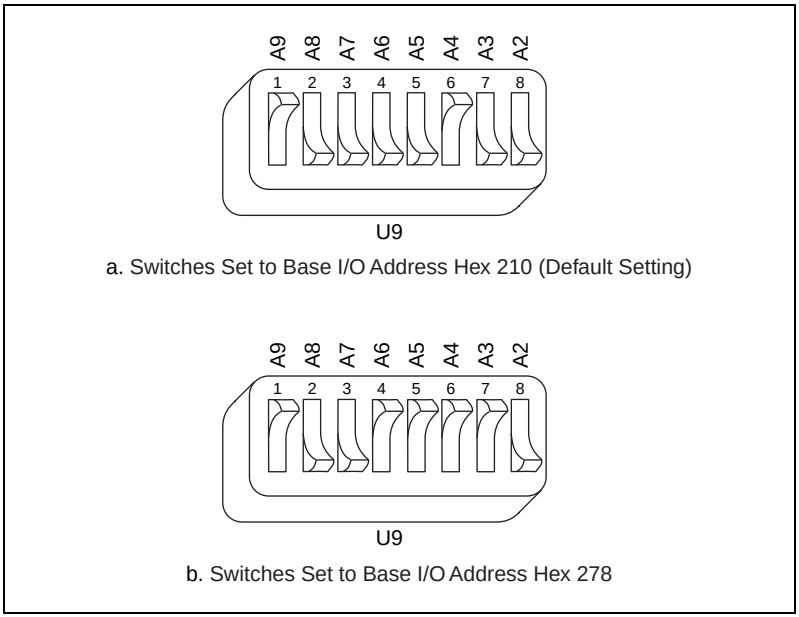


Figure D-2. Example Base I/O Address Switch Settings

Table D-3 shows some examples of switch settings and their corresponding address ranges.

Table D-3. Example Switch Settings with Corresponding Base I/O Address and I/O Address Space

Switch Setting								Base I/O Address (hex)	I/O Address Space Used (hex)
A9	A8	A7	A6	A5	A4	A3	A2		
0	1	0	0	0	0	0	0	100	100–103
0	1	0	0	1	0	0	0	120	120–123
0	1	0	1	0	0	0	0	140	140–143
0	1	0	1	1	0	0	0	160	160–163
0	1	1	0	0	0	0	0	180	180–183
0	1	1	0	1	0	0	0	1A0	1A0–1A3
0	1	1	1	0	0	0	0	1C0	1C0–1C3
0	1	1	1	1	0	0	0	1E0	1E0–1E3
1	0	0	0	0	0	0	0	200	200–203
1	0	0	0	1	0	0	0	220	220–223
1	0	0	1	0	0	0	0	240	240–243
1	0	0	1	1	0	0	0	260	260–263
1	0	1	0	0	0	0	0	280	280–283
1	0	1	0	1	0	0	0	2A0	2A0–2A3
1	0	1	1	0	0	0	0	2C0	2C0–2C3
1	0	1	1	1	0	0	0	2E0	2E0–2E3
1	1	0	0	0	0	0	0	300	300–303

Note: Base I/O address values 000 through 0FF hex are reserved for system use. Base I/O address values 100 through 3FF hex are available on the I/O channel.

Interrupt Selection

There are two sets of jumpers for interrupt selection on the PC-DIO-24 board. W3 is used for selecting the interrupt enable line. W2 is for selecting the interrupt level. The location of these jumpers is shown in Figure D-1.

Interrupt Enable Settings

To enable interrupt requests from the PC-DIO-24, you must set jumper W3 to select PC2, PC4, or PC6 as the active low interrupt enable line. When the interrupt enable line is logic low, interrupts are enabled from the PC-DIO-24 board. Refer to Chapter 4, *Theory of Operation*, for the suggested interrupt enable line setting for each digital I/O mode of operation. If W3 is set to N/C, all interrupt requests from the PC-DIO-24 are disabled. Figure D-3 shows the possible jumper settings for W3. The board ships with this jumper set to PC4; therefore, interrupt requests from the board are enabled and controlled by PC4.

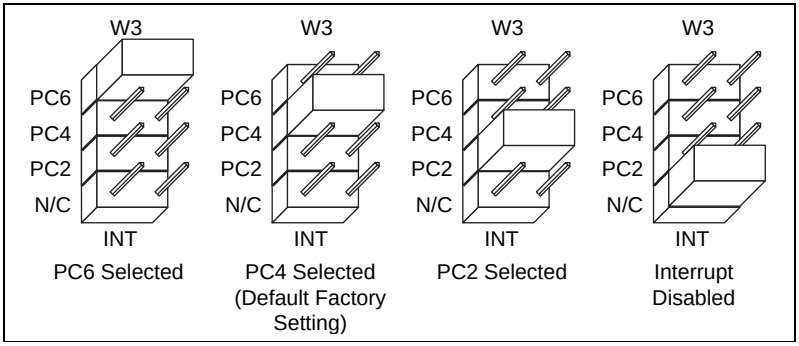


Figure D-3. Interrupt Enable Jumper Settings

Interrupt Level Settings

The PC-DIO-24 board can connect to any one of the six interrupt lines of the PC I/O Channel: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, or IRQ9. You select the interrupt line by setting a jumper on W2. To use the interrupt capability of the board, select an interrupt line and place the jumper in the appropriate position. The default interrupt line is IRQ5. To change to another line, remove the jumper from IRQ5 and place it on the pins for another request line. Figure D-4 shows the default factory setting for IRQ5.

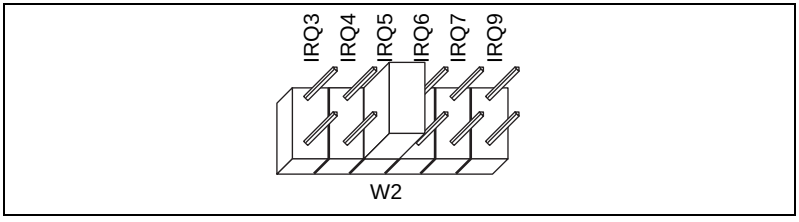


Figure D-4. Interrupt Jumper Setting for IRQ5 (Factory Setting)

The PC-DIO-24 uses a tristate driver to drive its selected interrupt line. The PC-DIO-24 can therefore share an interrupt line if your system and your other devices allow.

Installation

Install the PC-DIO-24 as described in Chapter 2, *Installation and Configuration*.

If you have an ISA-class computer and you are using a configurable software package, such as NI-DAQ, you may need to reconfigure your software to reflect any changes in jumper or switch settings. If you have an EISA-class computer, you need to update the computer resource allocation (or configuration) table by reconfiguring your computer. See your computer user manual for information about updating the configuration table.

Customer Communication

Appendix E

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

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National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call 512 795 6990. You can access these services at:

United States: 512 794 5422
Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

United Kingdom: 01635 551422
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

France: 01 48 65 15 59
Up to 9,600 baud, 8 data bits, 1 stop bit, no parity

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`support@natinst.com`

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Belgium	02 757 00 20	02 757 03 11
Brazil	011 288 3336	011 288 8528
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Québec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 6120092	03 6120095
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
United Kingdom	01635 523545	01635 523154
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Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___)_____ Phone (___) _____

Computer brand _____ Model _____ Processor_____

Operating system (include version number) _____

Clock speed _____MHz RAM _____MB Display adapter _____

Mouse ___yes ___no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

_____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem:_____

_____

_____

_____

_____

_____

PC-DIO-24/PnP Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

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Base I/O address of hardware _____

Programming choice _____

National Instruments application software version _____

Other boards in system _____

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Other Products

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Prefix	Meanings	Value
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

Symbols

°	degrees
–	negative of, or minus
Ω	ohms
/	per
%	percent
+	positive of, or plus

A

A	ampere
AC	alternating current
address	character code that identifies a specific location (or series of locations) in memory
AWG	American Wire Gauge

B

b	bit—one binary digit, either 0 or 1
B	byte—eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
base address	a memory address that serves as the starting address for programmable registers busthe group of conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the ISA and PCI bus. All other addresses are located by adding to the base address.
BCD	binary-coded decimal

C

C	Celsius
channel	pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.

D

D/A	digital-to-analog data acquisition—(1) collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing; (2) collecting and measuring the same kinds of electrical signals with A/D and/or DIO boards plugged into a computer, and possibly generating control signals with D/A and/or DIO boards in the same computer
DC	direct current
digital port	*See* port.
DIO	digital input/output
DMA	direct memory access

F

ft.	feet

H

h	hour
handshaked digital I/O	a type of digital acquisition/generation where a device or module accepts or transfers data after a digital pulse has been received. Also called latched digital I/O.
hardware	the physical components of a computer system, such as the circuit boards, plug-in boards, chassis, enclosures, peripherals, and cables
hex	hexadecimal
Hz	hertz—the number of scans read or updates written per second

I

in.	inches
Iin	input current
Iout	output current
interrupt	a computer signal indicating that the CPU should suspend its current task to service a designated activity
interrupt level	the relative priority at which a device can interrupt
I/O	input/output—the transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces
IRQ	interrupt request

K

k	kilo—the standard metric prefix for 1,000, or 10^3, used with units of measure such as volts, hertz, and meters

K	kilo—the prefix for 1,024, or 2^{10}, used with B in quantifying data or computer memory
kbytes	1,024 bytes
kbytes/s	a unit for data transfer that means 1,000 or 10^3 bytes/s

L

LabVIEW	laboratory virtual instrument engineering workbench
LSB	least significant bit

M

m	meters
M	(1) Mega, the standard metric prefix for 1 million or 10^6, when used with units of measure such as volts and hertz; (2) mega, the prefix for 1,048,576, or 2^{20}, when used with B to quantify data or computer memory
MB	megabytes of memory
MSB	most significant bit

N

NI-DAQ	National Instruments driver software for DAQ hardware

O

operating system	base-level software that controls a computer, runs programs, interacts with users, and communicates with installed hardware or peripheral devices

P

PPI	programmable peripheral interface

PnP	PnP (Plug and Play) refers to a device that is fully compatible with the industry standard Plug and Play ISA Specification. All bus-related configuration is performed through software, freeing you from manually configuring jumpers or switches to set the device base address and interrupt level. PnP systems automatically arbitrate and assign system resources to a PnP product.
port	(1) a communications connection on a computer or a remote controller (2) a digital port, consisting of four or eight lines of digital input and/or output

R

RAM	random-access memory
resolution	the smallest signal increment that can be detected by a measurement system. Resolution can be expressed in bits, in proportions, or in percent of full scale. For example, a system has 12-bit resolution, one part in 4,096 resolution, and 0.0244% of full scale.
R_{EXT}	external resistance

S

s	seconds
S	samples
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy PC environment
signal conditioning	the manipulation of signals to prepare them for digitizing
S/s	samples per second—used to express the rate at which a DAQ board samples an analog signal
SSR	solid-state relay

V

V	volts
Vcc	Supply voltage; for example, the voltage a computer supplies to its plug-in devices
VDC	volts direct current
V_{EXT}	external volt
VI	virtual instrument—(1) a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic stand-alone instrument (2) a LabVIEW software module (VI), which consists of a front panel user interface and a block diagram program

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Special Characters

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